PHYSICS AND TECHNOLOGY OF CRYSTALLINE OXIDE SEMICONDUCTOR CAAC-IGZO

APPLICATION TO DISPLAYS

Edited by

Shunpei Yamazaki and Tetsuo Tsutsui

WILEY SID Series in Display Technology

PHYSICS AND TECHNOLOGY OF CRYSTALLINE OXIDE SEMICONDUCTOR CAAC-IGZO

Wiley-SID Series in Display Technology

Series Editors:
Anthony C. Lowe and Ian Sage

Display Systems: Design and Applications
Lindsay W. MacDonald and Anthony C. Lowe (Eds.)

Electronic Display Measurement: Concepts, Techniques, and Instrumentation
Peter A. Keller

Reflective Liquid Crystal Displays
Shin-Tson Wu and Deng-Ke Yang

Colour Engineering: Achieving Device Independent Colour
Phil Green and Lindsay MacDonald (Eds.)

Display Interfaces: Fundamentals and Standards
Robert L. Myers

Digital Image Display: Algorithms and Implementation
Gheorghe Berbecel

Flexible Flat Panel Displays
Gregory Crawford (Ed.)

Polarization Engineering for LCD Projection
Michael G. Robinson, Jianmin Chen, and Gary D. Sharp

Introduction to Microdisplays
David Armitage, Ian Underwood, and Shin-Tson Wu

Mobile Displays: Technology and Applications
Achintya K. Bhowmik, Zili Li, and Philip Bos (Eds.)

Photoalignment of Liquid Crystalline Materials: Physics and Applications
Vladimir G. Chigrinov, Vladimir M. Kozenkov, and Hoi-Sing Kwok

Projection Displays, Second Edition
Matthew S. Brennesholtz and Edward H. Stupp

Introduction to Flat Panel Displays
Jiun-Haw Lee, David N. Liu, and Shin-Tson Wu

LCD Backlights
Shunsuke Kobayashi, Shigeo Mikoshiba, and Sungkyoo Lim (Eds.)

Liquid Crystal Displays: Addressing Schemes and Electro-Optical Effects, Second Edition
Ernst Lueder

Transflective Liquid Crystal Displays
Zhibing Ge and Shin-Tson Wu

Liquid Crystal Displays: Fundamental Physics and Technology
Robert H. Chen

3D Displays
Ernst Lueder

OLED Display Fundamentals and Applications
Takatoshi Tsujimura

Illumination, Color and Imaging: Evaluation and Optimization of Visual Displays
Peter Bodrogi and Tran Quoc Khanh

Interactive Displays: Natural Human-Interface Technologies
Achintya K. Bhowmik (Ed.)

Addressing Techniques of Liquid Crystal Displays
Temkar N. Ruckmongathan

Fundamentals of Liquid Crystal Devices, Second Edition
Deng-Ke Yang and Shin-Tson Wu

Modeling and Optimization of LCD Optical Performance
Dmitry A. Yakovlev, Vladimir G. Chigrinov, and Hoi-Sing Kwok

PHYSICS AND TECHNOLOGY OF CRYSTALLINE OXIDE SEMICONDUCTOR CAAC-IGZO

APPLICATION TO DISPLAYS

Edited by

Shunpei Yamazaki
Semiconductor Energy Laboratory Co., Ltd, Japan

Tetsuo Tsutsui
Kyushu University (Professor Emeritus), Japan

WILEY

This edition first published 2017

Registered Office
John Wiley & Sons, Ltd, The Atrium, Southern Gate, Chichester, West Sussex, PO19 8SQ, United Kingdom

For details of our global editorial offices, for customer services and for information about how to apply for permission to reuse the copyright material in this book please see our website at www.wiley.com.

Library of Congress Cataloging-in-Publication Data

Names: Yamazaki, Shunpei, 1942– | Tsutsui, Tetsuo, 1944–
Title: Physics and technology of crystalline oxide semiconductor CAAC-IGZO. Application to displays / Shunpei Yamazaki, Tetsuo Tsutsui.
Description: Chichester, West Sussex, United Kingdom : John Wiley & Sons, Inc., 2017. | Series: Wiley-SID series in display technology | Includes index.
Identifiers: LCCN 2016034591 | ISBN 9781119247456 (cloth) | ISBN 9781119247449 (ePDF) | ISBN 9781119247487 (ePub)
Subjects: LCSH: Semiconductors–Materials. | Semiconductors–Characterization. | Gallium compounds. | Zinc compounds. | Oxides. | Electroluminescent display systems–Materials.
Classification: LCC TK7871.85 .Y357597 2017 | DDC 621.3815/20284–dc23
LC record available at https://lccn.loc.gov/2016034591

A catalogue record for this book is available from the British Library.

Set in 10/12pt Times by SPi Global, Pondicherry, India

10 9 8 7 6 5 4 3 2 1

Contents

About the Editors

Shunpei Yamazaki received his Ph.D., ME, BE, and honorary degrees from Doshisha University, Japan, in 1971, 1967, 1965, and 2011, respectively, and is the founder and president of Semiconductor Energy Laboratory Co., Ltd. He invented a basic device structure of non-volatile memory known as “flash memory” in 1970 during his Ph.D. program. Yamazaki is a distinguished foreign member of the Royal Swedish Academy of Engineering Sciences and a founder of Kato & Yamazaki Educational Foundation. Yamazaki has published or co-published over 400 papers and conference presentations and is the inventor or co-inventor of over 6314 patents (Guinness World Record in 2011).

1967	Completed Master’s Degree Program at Doshisha University Graduate School of Engineering
1970	Invented a basic device of flash memory (Japanese Patent No. 886343; Japanese Examined Patent Application Publication No. Sho50-36955)
1971	Received Ph.D. in Engineering from Doshisha University Graduate School Doctoral Program Joined TDK Corporation (formerly TDK Electronics Co., Ltd.)
1980	Established Semiconductor Energy Laboratory Co., Ltd. and assumed position as president
1984	Awarded the Richard M. Fulrath Award by the American Ceramic Society (for research on MIS structure)
1995	Awarded the Medal with Dark Blue Ribbon from the Cabinet Office of the Japanese government (proceeds given to Japanese Red Cross Society) (awarded 6 times since 2015)
1997	Awarded the Medal with Purple Ribbon from the Cabinet Office of the Japanese government (for development of MOS LSI element technology)
2009	IVA (Royal Swedish Academy of Engineering Science) Foreign Member
2010	Awarded Okochi Memorial Technology Award from Okochi Memorial Foundation

2011 IEEE Life Fellow
Received Honorary Doctor Degree of Culture from Doshisha University
Renewed his first Guinness World Record in 2004 (man holding the most patents in the world)
2015 Granted the title of "Friend of Doshisha" by Doshisha University
SID Special Recognition Award for "discovering CAAC-IGZO semiconductors, leading their practical application, and paving the way to next-generation displays by developing new information-display devices such as foldable or 8 K × 4 K displays".

Tetsuo Tsutsui received his BS (1967) and MS (1969) in Applied Chemistry from Kyushu University, Japan, and Dr. of Engineering in Materials Science from the Graduate School of Engineering Sciences of the same university in 1977. He was a professor at the Graduate School of Engineering Sciences, Kyushu University from 1986 to 2008. His research interests are in the electronic and optical properties of molecular solids and organic semiconductor electronics, including organic light-emitting diodes, organic FETs, and organic photovoltaic devices. He has published more than 200 original and 50 review papers. He received the Polymer Society Award (Polymer Society, Japan, 1995), Chemical Society of Japan Award (2008), Medal with Purple Ribbon (Cabinet Office of the Japanese Government, 2009), and Jan Rajchman Prize (Society for Information Displays, 2011). He is a Fellow of the Japan Society of Applied Physics and a Professor Emeritus at Kyushu University.

1967 Completed Bachelor of Engineering at Department of Applied Chemistry, Faculty of Engineering, Kyushu University
1969 Completed Master of Engineering at Department of Applied Chemistry, Graduate School of Engineering, Kyushu University
1971 Research Associate at Faculty of Engineering, Kyushu University
1978 Received Doctor of Engineering on Materials Science, Kyushu University
1980 Research Associate at Graduate School of Engineering Sciences, Kyushu University
1986 Associate Professor at Graduate School of Engineering Sciences, Kyushu University
1995 Professor at Faculty of Engineering Sciences, and Graduate School of Engineering Sciences, Kyushu University
2003 Dean of Faculty of Engineering Sciences, and Graduate School of Engineering Sciences, Kyushu University
2006 Professor at Institute for Materials Chemistry and Engineering, and Graduate School of Engineering Sciences, Kyushu University
2007 Awarded the Fellow of Japan Applied Physics Society
2008 Retired from Kyushu University, and honored to Professor Emeritus, Kyushu University
2008 Research Fellow at Semiconductor Energy Laboratory Co. Ltd.
2010 Senior Manager of Management Office at Organic Photonics and Electronics Research Center (OPERA), Kyushu University
2011 Senior vice President at Chemical Materials Evaluation and Research Base (CEREBA)
2011 Awarded the Jan Rajchman Prize (Society for Information Display)

List of Contributors

Shunpei Yamazaki (editor)	Semiconductor Energy Laboratory Co., Ltd.
Tetsuo Tsutsui (editor)	Kyushu University (Professor Emeritus)

In alphabetical order:

Shingo Eguchi	Semiconductor Energy Laboratory Co., Ltd.
Takashi Hamochi	Advanced Film Device Inc.
Yoshiharu Hirakata	Semiconductor Energy Laboratory Co., Ltd.
Ryunosuke Honda	Semiconductor Energy Laboratory Co., Ltd.
Yasuharu Hosaka	Advanced Film Device Inc.
Hisao Ikeda	Semiconductor Energy Laboratory Co., Ltd.
Tetsuji Ishitani	Semiconductor Energy Laboratory Co., Ltd.
Masahiro Katayama	Semiconductor Energy Laboratory Co., Ltd.
Kiyotaka Kimura	Semiconductor Energy Laboratory Co., Ltd.
Hidetomo Kobayashi	Semiconductor Energy Laboratory Co., Ltd.
Junichi Koezuka	Semiconductor Energy Laboratory Co., Ltd.
Daisuke Kubota	Semiconductor Energy Laboratory Co., Ltd.
Daisuke Kurosaki	Advanced Film Device Inc.
Koji Kusunoki	Semiconductor Energy Laboratory Co., Ltd.
Shinpei Matsuda	Semiconductor Energy Laboratory Co., Ltd.
Hiroyuki Miyake	Semiconductor Energy Laboratory Co., Ltd.
Yasutaka Nakazawa	Advanced Film Device Inc.
Toshimitsu Obonai	Advanced Film Device Inc.
Kenichi Okazaki	Semiconductor Energy Laboratory Co., Ltd.
Satoru Saito	Semiconductor Energy Laboratory Co., Ltd.
Satoshi Seo	Semiconductor Energy Laboratory Co., Ltd.
Yukinori Shima	Advanced Film Device Inc.
Hideaki Shishido	Semiconductor Energy Laboratory Co., Ltd.
Tsunenori Suzuki	Semiconductor Energy Laboratory Co., Ltd.
Kei Takahashi	Semiconductor Energy Laboratory Co., Ltd.

Kazunori Watanabe Semiconductor Energy Laboratory Co., Ltd.
Roh Yamamoto Semiconductor Energy Laboratory Co., Ltd.
Kohei Yokoyama Semiconductor Energy Laboratory Co., Ltd.

Series Editor's Foreword

From 2003 onward when IGZO TFTs were first developed, this transparent semiconductor technology has aroused huge interest for display applications. In 2012 the first products entered the market, and since then oxide-based active matrix displays have made spectacular progress, as evidenced by the demonstration of devices with ever-increasing size and complexity. Especially in the field of high-resolution displays, IGZO backplane devices have matched and then exceeded the capabilities of other thin-film technologies. Meanwhile, oxide active matrix displays have realized unique advances in areas such as power saving through slow refresh rates and improved aperture ratios.

The present book provides a comprehensive view of the application of one form of oxide semiconductor – the *c*-axis-aligned crystal (CAAC) form – to displays. The high mobility (compared with more traditional α-Si), extremely low leakage current, and relative immunity from short-channel effects in CAAC oxide TFTs allows them to provide all the advantages outlined above, and allows integration of gate-driver circuits on the display, providing extremely narrow bezel widths. The different TFT structures which can be applied to CAAC oxide devices are described, together with their fabrication process flows and resulting properties, as well as an account of different pixel and driver circuits.

In addition to accounts of AM backplane technologies and driver architectures, other topics of central importance to exploiting these advantages are detailed. One is the use of oxide-doped organic materials as hole-injection layers in OLEDs. The resulting layers are highly conductive and can be made thick to increase the yield and reliability of OLED structures, without increasing the drive voltage. A second technology is the fabrication of flexible OLEDs through the use of tungsten release layers; this approach is complementary to the ability of CAAC AM layers to withstand flexing without alteration of their switching properties, and provides a basis for scalable manufacture of flexible OLED devices.

In this book, together with its companion volumes on CAAC oxide *Fundamentals* and on *Applications to LSI*, the editors and authors provide an account of CAAC-oxide semiconductors which will be invaluable to those seeking to exploit or understand the field, spanning as it does the whole subject from deposition conditions and structural studies, to the fabrication process flow for complete displays. Dr. Yamazaki and his colleagues bring unrivalled research experience and enthusiasm to their treatment of the subject, to provide a comprehensive and approachable description.

Ian Sage
Malvern, 2016

Preface

Entering the 21st century, it seems that the growth of the electronics industry, one of the largest industries in the world, is hitting a growth saturation level. That is because the amount of energy used by people, which has already become enormous, as reflected in the abrupt climate change in recent years, is going to increase even more with its growth. Especially, the energy consumption of cloud computing and electronic devices such as smartphones and supercomputers will continue to increase. Therefore, it is not an exaggeration to say that the development of new energy-saving devices has a direct influence on the continued existence of all mankind.

For this reason, we started extensive research on crystalline oxide semiconductors (OSs), especially on a *c*-axis-aligned crystalline indium–gallium–zinc oxide (CAAC-IGZO) semiconductor. Owing to the economic downturn in the aftermath of the Lehman Brothers bankruptcy in the autumn of 2008, many companies withdrew from research on this subject, but I never gave up and our research has continued to the present day. One of the most important characteristics of a field-effect transistor (FET) using this wide-gap semiconductor is that the off-state current is on the order of yA/cm (10^{-24}A/cm) (where yocto is the smallest SI prefix), which is smaller than that of any other device measured so far. This characteristic effectively reduces the energy consumption, and thus we believe that it coincides with society's need to save energy.

It has been less than 10 years since I started researching and developing oxide semiconductors, but I think that proposing their effectiveness without delay is the first step toward a contribution to humanity. That is why I would like to introduce this book series *Physics and Technology of Crystalline Oxide Semiconductor*, consisting of *Fundamentals*, *Application to LSI*, and *Application to Displays*, even though I know that it cannot be said that every detail is completely covered in the book series.

The book series contains the discovery of CAAC-IGZO by me, Shunpei Yamazaki, one of the editors and authors thereof, as well as research results on its application obtained at Semiconductor Energy Laboratory Co., Ltd. (SEL), where I serve as president. We have decided to write the experimental facts down in as much detail as possible, and publish models whose principles have yet to be verified. The reason is that I would like to give a couple of hints to our readers – such as graduate students, on-site researchers, and developers – as soon as possible, so that they can conduct further R&D. For these reasons, as well as the limited number of pages, I would like you to accept my deepest apologies for not being able to publish all of the data in these books. Even after the publication of these three books about crystalline oxide semiconductors, I would like to continue making our CAAC-IGZO technology known to the public by conducting further research from both an engineering and an academic point of view.

This book presents various topics on CAAC-IGZO applications to display technologies, which enable displays with low power consumption, flexible displays, and next-generation organic light-emitting diode (OLED) displays.

In the past, the Bell Laboratories published a set of books called *The Bell Telephone Laboratories series* about the invention of transistors and research results thereof, which accordingly spread the current concept of transistors throughout the world. We sincerely hope that our books will help to spread the CAAC-IGZO technology, just as *The Bell Telephone Laboratories series* helped to popularize the concept of transistors. I think that CAAC-OS, especially CAAC-IGZO, still has many unexplored possibilities, and thus more institutions and scientists should research it in cooperation with each other. I am expecting that the CAAC-IGZO which we discovered will flourish in the 21st century, by publishing its physical properties and principles as well as by applying it in the display and LSI fields, especially applying it to energy-saving devices.

So far, we have made some efforts by submitting papers and giving presentations at various conferences about crystalline oxide semiconductors and OS FETs. However, we have never heard about any case where a ceramic material was used for the active element on a mass-production basis in Si LSI or displays; thus, many companies, with the exception of Sharp Corporation, will face difficulties in terms of mass production. Note that a ceramic with an amorphous structure has been proposed before, but it was not put into practical use due to reliability problems. In particular, the depression following 2008 made many companies quit their R&D of ceramics with an amorphous structure; it was deemed fruitless, because FETs utilizing amorphous ceramics lack reliability. The actual reasons are that many oxygen vacancies (V_O) as well as hydrogenated oxygen vacancies generated by hydrogen trapped in V_O exist in a less crystallized IGZO.

I observed a transmission electron microscopy (TEM) image of an IGZO film in front of a TEM screen to find a solution for the reliability issue. At that time, I discovered that a CAAC structure existed in the IGZO film. I thought that the problem of reliability could be solved by the use of this kind of material, and thus shifted the focus of our R&D to CAAC-IGZO. A FET using this CAAC-IGZO has a high level of reliability, which cannot be said about FETs which use amorphous IGZO. Thus, a FET with a CAAC-IGZO is excellent from a repeatability point of view, in that it can be measured and evaluated stably, both at the material and device level. As a result of the stable measurement and evaluation, we discovered that the off-state current is on the order of yA/cm (10^{-24}A/cm), as mentioned above. Additionally, since IGZO has a wide solid-solution phase, we succeeded in fabricating FETs using CAAC-IGZOs having high mobilities of 30–70 cm^2/V-s, thus exceeding 50 cm^2/V-s, by changing the composition ratio and the device structure. A mobility equaling that of an LTPS-FET means that the CAAC-IGZO might be able to not only fight evenly with an LTPS-FET but also outperform it in the industry. Furthermore, we tried to apply CAAC-IGZO FETs to LSI, something which has never been done before, and discovered that such a FET can operate with a channel length of just 20–60 nm, while such a short channel causes short-channel effects in Si FETs.

Our data has been reviewed by many specialists, but it seems that to help people understand *the true value of the crystalline oxide semiconductor*, there is still a need to further explain the numerous issues concerning fundamental properties, which have not yet been fully understood. Moreover, a lot of people gave us the same advice: to help intellectuals grasp the whole picture of the technology by publishing a series of at least three books (*Fundamentals*, *Application to LSI*, and *Application to Displays*). Accordingly, I decided to publish them. Note that most of the content of these books is based on our experimental data. Hence, please acknowledge SEL and Advanced Film Device Inc. (AFD Inc), a subsidiary of SEL, as the sources of these books, unless otherwise specified.

After we started planning the book series on CAAC-IGZO, SEL progressed significantly in R&D on crystalline oxide semiconductors, which were not included in the criterion of CAAC-IGZO. Now we understand that the world of science and technology on crystalline oxide semiconductors is expanding wider and deeper beyond the CAAC-IGZO presented in this book series. I would be very happy if we could introduce you to our expanded and enriched visions on crystalline oxide semiconductors in a revised and enlarged edition of this book series in the near future.

During the creation of this book, many people helped and guided us. We would like to express our sincere gratitude especially to Dr. Tetsuo Tsutsui for being a co-editor of this book, *Application to Displays*. Dr. Tsutsui has given us instruction regarding OLED research for more than 17 years. During that period, he has exerted himself to educate many of our research members as a corporate advisor. He has also given us opportunities for joint research with other institutions on organic compounds having a tandem or hybrid structure. I am really grateful that Dr. Tsutsui kindly accepted the position of director of this book.

Moreover, during the R&D on which these books are based, as well as during the writing process, many young researchers at SEL also contributed. Their names appear in the list of contributors.

We would also like to extend our heartfelt thanks to Dr. Johan Bergquist, Dr. Tadashi Akabane, Dr. Michio Tajima, and Mr. Jun Koyama for helping us with the English translation of this book, checking errors, and giving us a great deal of advice on how to improve our text.

I have been blessed with support and cooperation from many outstanding individuals. I would like to add that I could not have finished these books in such a short period of time without the efforts of Dr. Ian Sage, Wiley-SID book series editor, who suggested the publication of the books, as well as Ms. Alexandra Jackson, Ms. Ella Mitchell, and Ms. Nithya Sechin of John Wiley & Sons, Limited. Last but not least, I would like to express my sincere gratitude to the publishers and authors for allowing us to use their figures as references in these books.

Shunpei Yamazaki
President of Semiconductor Energy Laboratory Co., Ltd.

Acknowledgments

First of all, we would like to thank **Dr. Johan Bergquist**, **Dr. Tadashi Akahane**, **Dr. Michio Tajima**, and **Mr. Jun Koyama**, who encouraged us and gave valuable advice on writing manuscripts.

Furthermore, we would also like to thank many people in a variety of fields for providing data, cooperation in writing manuscripts and English translation, and all other aspects of this book.

Our heartfelt thanks to (in alphabetical order):

Technical support

Mr. Kanta Abe	Mr. Tomoya Aoyama	Mr. Haruyuki Baba
Mr. Akihiro Chida	Mr. Yoshitaka Dozen	Mr. Masakazu Egawa
Mr. Takao Hamada	Mr. Toshiki Hamada	Dr. Naoaki Hashimoto
Ms. Kaoru Hatano	Mr. Ryo Hatsumi	Mr. Shinichi Hirasa
Ms. Nozomi Horikoshi	Dr. Shunsuke Hosoumi	Mr. Satoru Idojiri
Mr. Satoshi Ikezoe	Ms. Hideko Inoue	Ms. Seiko Inoue
Mr. Toshiyuki Isa	Mr. Fumito Isaka	Ms. Ayumi Ishigaki
Mr. Takashi Ishizaka	Mr. Minato Ito	Mr. Yuji Iwaki
Mr. Yasuhiro Jinbo	Mr. Hiroshi Kadoma	Mr. Taisuke Kamata
Ms. Miki Kanamoto	Mr. Masatoshi Kataniwa	Mr. Sho Kato
Mr. Takahiro Kawakami	Mr. Hiromitsu Kido	Mr. Hajime Kimura
Mr. Yasushi Kitano	Mr. Manabu Kobayashi	Mr. Ryu Komatsu
Mr. Yusuke Kubota	Ms. Noriko Matsumoto	Ms. Satomi Mitsumori
Mr. Hidenori Mori	Ms. Hiroko Murata	Mr. Takaaki Nagata
Mr. Daiki Nakamura	Ms. Harue Nakashima	Mr. Masataka Nakata
Mr. Ryo Nakazato	Mr. Yasuhiro Niikura	Mr. Yusuke Nishido
Dr. Ryoji Nomura	Mr. Yusuke Nonaka	Ms. Hiromi Nowatari
Ms. Kaori Ogita	Ms. Yuko Ohe	Mr. Masakatsu Ohno
Mr. Naoto Ohno	Ms. Eriko Ohomori	Mr. Nobuharu Ohsawa

Mr. Satoru Ohshita
Mr. Takeshi Osada
Ms. Sayaka Sanefuji
Mr. Keita Sato
Ms. Satoko Shitagaki
Mr. Hiroki Suzuki
Mr. Tatsuyoshi Takahashi
Mr. Kouhei Toyotaka
Mr. Shogo Uesaka
Mr. Masaaki Watanabe
Mr. Tomoya Yamaguchi
Ms. Ikumi Yamazaki
Mr. Shota Yatsuzuka
Mr. Tatsuya Okano
Mr. Junichiro Sakata
Mr. Takeru Sasaki
Mr. Takehisa Sato
Mr. Yui Suematsu
Mr. Kunihiko Suzuki
Mr. Yusuke Takita
Mr. Kazuki Tsuda
Mr. Takahiro Ushikubo
Mr. Yui Yamada
Mr. Ryohei Yamaoka
Mr. Yuichi Yanagisawa
Mr. Koji Ono
Mr. Tatsuya Sakuishi
Mr. Toshiki Sasaki
Ms. Hitomi Shionoya
Mr. Nozomu Sugisawa
Mr. Masato Suzuki
Mr. Yuki Tamatsukuri
Mr. Yutaka Uchida
Mr. Takeyoshi Watabe
Ms. Sachiko Yamagata
Mr. Akio Yamashita
Mr. Seiji Yasumoto

Other support

Ms. Mayumi Adachi
Mr. Koji Dairiki
Mr. Takahiro Kanda
Mr. Masumi Kuwabara
Mr. Hasumi Nomaguchi
Mr. Takashi Shingu
Ms. Mika Tatsumi
Ms. Hitomi Tsurui
Mr. Kensuke Yoshizumi
Ms. Yukari Amano
Ms. Ai Hattori
Mr. Masayuki Kimura
Ms. Michiyo Mashiyama
Ms. Yoko Otake
Ms. Tamae Takano
Mr. Yosuke Tsukamoto
Ms. Chiaki Yamura
and many others
Mr. Tobias Breitling
Ms. Yasuko Iharakumi
Ms. Yuko Konno
Ms. Tomoko Nakagawa
Ms. Yu Sasaki
Mr. Toru Takayama
Ms. Hisako Tsukiki
Ms. Naomi Yazaki

Shunpei Yamazaki
Tetsuo Tsutsui

1

Introduction

Field-effect transistors (FETs) are developed using various semiconductor materials, the most common of which is silicon (Si). FETs are employed in many products and lead to performance improvements and reductions in size and weight, with increasing miniaturization. The extraordinary progress in the Si FET technology used in both large-scale integrated circuits (LSIs) and flat-panel displays has a tremendous impact on lifestyles. Several players continue to be engaged in the fierce race to further develop Si FET technology. Meanwhile, device power consumption continues to increase, and lowering the power consumption has become necessary for various applications, such as the Internet of Things (IoT) and wearable applications.

Given these circumstances, crystalline oxide semiconductors (crystalline OS) draw much attention for their ability to reduce power consumption in electronic circuits. IGZO has been particularly studied in detail, and its fundamental properties have been examined to develop its applications for products. The discovery of a unique class of crystalline OS, the *c*-axis-aligned crystalline IGZO (CAAC-IGZO), is a key finding of these studies.

Physics and Technology of Crystalline Oxide Semiconductor CAAC-IGZO documents the research and developments reported by S. Yamazaki and colleagues to date. It consists of three volumes, namely *Fundamentals*, *Application to LSI*, and *Application to Displays* (Figure 1.1). *Fundamentals* introduces oxide semiconductor materials, crystal structure analysis, the fundamental properties and FET characteristics of CAAC-IGZO, and a comparison with Si FETs [1]. *Application to LSI* focuses on the applications of CAAC-IGZO to LSI devices, and describes the FET structures, fundamental electrical characteristics, nano-sized (e.g., 20-nm node) transistor prototypes, and examples of LSI applications, including non-volatile memory devices [2].

This volume, entitled *Application to Displays*, introduces approaches to fulfill the market demand for devices with further enhancements in image displays at lower costs and power

Physics and Technology of Crystalline Oxide Semiconductor CAAC-IGZO: Application to Displays, First Edition.
Edited by Shunpei Yamazaki and Tetsuo Tsutsui.

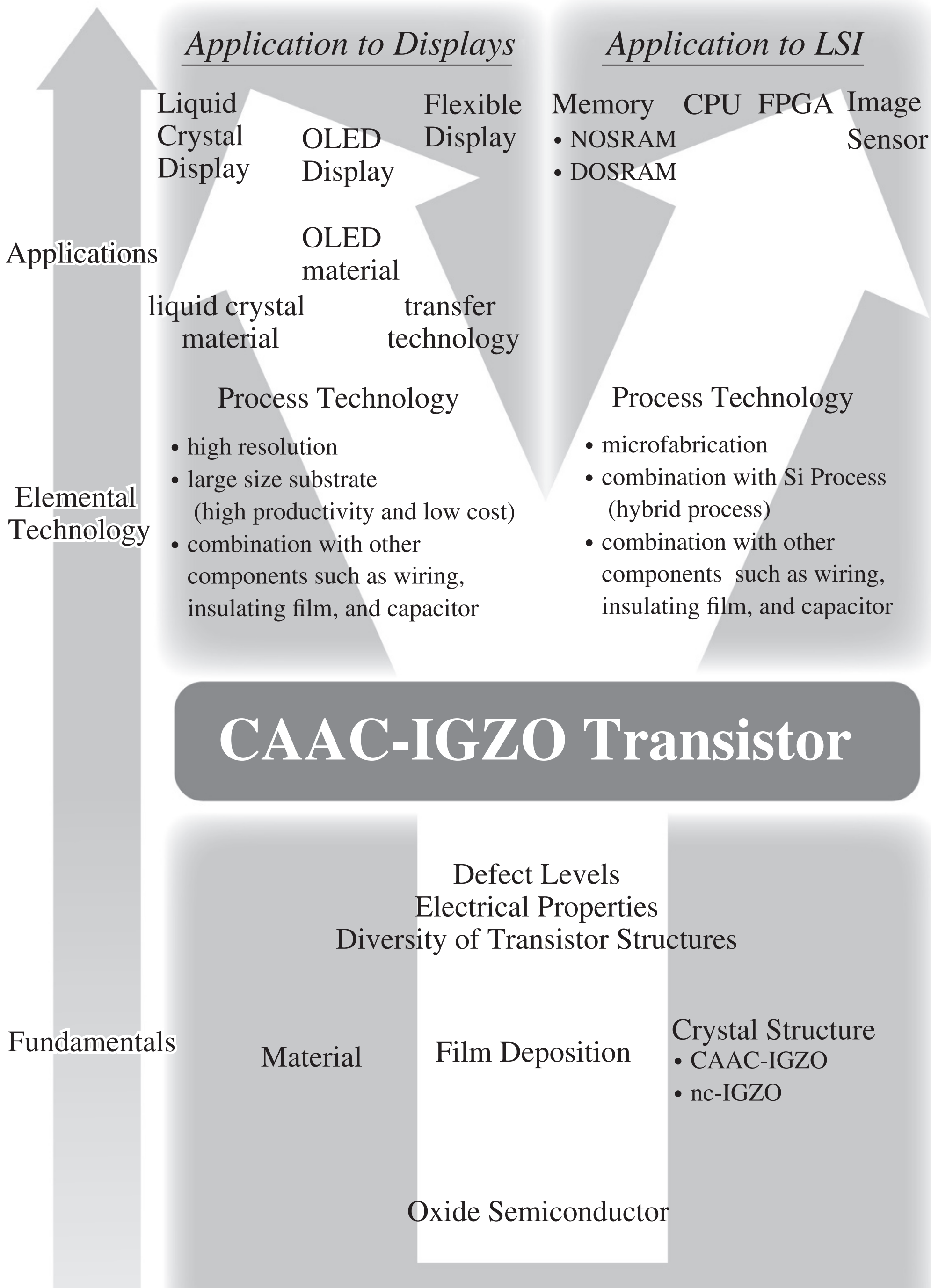


Figure 1.1 Framework of *Physics and Technology of Crystalline Oxide Semiconductor CAAC-IGZO*

consumption. In particular, it describes the CAAC-IGZO FET structure, manufacturing processes, FET characteristics, and circuit design. Subsequently, the organic light-emitting diode (OLED) display, a highly promising next-generation technology, is presented. In particular, the materials and elements for power-efficient operations are discussed in detail, along with the pixel structures for high-yield displays with a high pixel density.

This volume also introduces the fabrication method of flexible displays based on OLED displays, and proposes new possibilities for displays, sensors, and other devices. In addition, it presents a review of liquid crystal displays (LCDs), which are currently the most popular displays, from the point of view of providing high resolution and low power consumption.

Furthermore, the volume also discusses actual OLED displays with CAAC-IGZO FETs, LCD circuit designs, and display prototypes with a high pixel density.

1.1 History of Displays

For more than half a century, cathode-ray tubes (CRTs) were used to develop display devices for televisions (TVs) and monitors. However, the development and widespread use of LCDs [3] has replaced CRTs as they produce flat-panel displays that are thin, light, and have low power consumption. The earliest LCDs used in watches and calculators displayed monochrome alphanumeric characters in a small display area. Then, larger LCDs were developed and used in word processors, which displayed more characters and pictures. This was followed by laptop computers, which displayed more detailed color images. Next, pagers – as portable personal terminals – attracted the attention of companies and students, but were swiftly replaced by mobile phones. The first mobile phones could only display alphanumeric characters. Subsequently, mobile phones were developed to include integrated cameras capable of handling images, mapping data, and downloading audiovisual information from the Internet. As a result, larger color displays with an increased number of pixels appeared and resulted in displays with higher pixel densities.

The increasing number of pixels forced the LCDs to abandon a passive-matrix-driving method in favor of active-matrix (AM) driving [4], by incorporating a storage capacitor and thin-film transistors (TFTs) in each pixel. Additionally, the video display required a shorter display refresh period and this was another reason for the introduction of AM LCDs. The passive-matrix driving was slow, because of both the liquid crystal material response and the duty driving that could not retain the amount of rewriting required for gate lines in a limited period. There was also a limit on reducing the distance between pixels, because of the crosstalk between adjacent pixels. AM displays were popular, as they allowed high-speed refresh for video portrayal, because of the direct writing of video data into the storage capacitor through the pixel FET. Hence, fast data rewriting was possible even for a significantly large number of pixels without the need to wait for the refresh to complete. AM LCDs also ensured a large number of gray shades and high contrasts, because the gray levels were completely stored as an analog amount of charges written in the storage capacitor.

With the coming of the 21st century, large CRT TVs were eventually replaced by AM LCD TVs. Simultaneously, TV broadcasting moved from analog to digital, and full high-definition TVs (1920×1080) were widely adopted by the market. Currently, 4 K TVs (3840×2160), which are compatible with 4 K broadcasting, are being developed in mainstream markets. They will shortly be succeeded by 8 K broadcasting and 8 K TVs (7680×4320) [5, 6].

1.2 Requirement for Displays

Early AM LCD TV displays exhibited motion blurring as a result of the sample-and-hold addressing. Hence, many LCDs adopted black frame insertion (BFI) between video frames and/or backlight blinking to solve the problem of blurring. A refresh rate higher than 50/60 Hz, similar to CRTs, is thereby required to avoid flicker, which disappears at approximately 75–85 Hz. However, the broadcasting and video standards were sampled at 50 or 60 Hz (25 or 30 Hz interlaced) to avoid image tearing by doubling the chosen refresh rate, particularly in the case of 50 Hz CRTs. The AM LCDs with BFI or backlight blinking similarly doubled the refresh rate. Frame interpolation with constant backlight and without BFI was introduced, as they faced the issue of reduced luminance. Some products even adopted quadruple refresh rates.

To date, the pixel FETs in large displays, such as TVs and monitors, use amorphous silicon (a-Si) because of the mass-manufacturing compatibility for large glass substrates [7]. Unfortunately, the a-Si TFTs have low mobility and are not compatible with high-speed data writing in large screens with high resistive/capacitive (RC) loads. Therefore, the pixel numbers required for full high definition (1920 × 1080) are barely manageable with a-Si TFTs. Hence, other FET technologies are required for 4 K (3840 × 2160) and 8 K (7680 × 4320) displays, which exhibit much higher RC loads. Various attempts were made to reduce the loads. Examples of these include introducing copper wirings, dividing the driving by splitting the screen horizontally or vertically, inserting black frames by synchronizing the partition control of the backlights, and rewriting the image data. However, these approaches resulted in increased costs and also increased the power consumption of the control ICs and backlights.

The development of both cable and wireless Internet networks allows individuals to ubiquitously access information. This facilitated the transition from mobile phones to smartphones, and from laptops and desktop computers to tablet computers. The development of devices and infrastructures that could handle large amounts of data, such as high-bandwidth videos, has also contributed to this situation. Additionally, touch sensors revolutionized the human–machine interface (HMI) through increased interactivity. This also necessitated high-performance display devices.

For personal displays for virtual reality (VR) and augmented reality (AR) applications, the pixel density, cost, and power consumption are extremely challenging issues, particularly for the 8K format, so new solutions are necessary. There is also a growing trend of curved displays in, for example, automotive applications.

The key quality factors for high-performance displays include high contrast, excellent color reproduction, high resolution, and crisp and flicker-free moving images. In particular, displays viewed at a short distance require high resolution to avoid jaggedness.

The requirements for these displays depend on their use case and screen size. Small-display personal devices require particularly high pixel density and smaller FETs. For example, a pixel density of over 1000 PPI (for VR and AR applications) requires FETs with a channel length as short as 2–3 μm. This size cannot be achieved even by low-temperature polysilicon (LTPS), which is a FET technology widely used in current small-sized displays. Furthermore, the increase in the number of pixels also increases the number of gate lines and pixel data lines. Hence, higher-performance FETs are necessary in the driving and control circuits integrated on the display substrate. For example, when a display panel is synchronized with a touch sensor, a part of the display period is allocated to the sensor driving and read-out. Thus, the control FETs are required to be smaller and to be operated at higher speeds and higher currents. This in turn necessitates high mobility and on-state current. The small FETs also ensure a higher aperture ratio, which leads to a lower total power consumption for a given display luminance.

The above discussion is mainly applicable for LCDs, which are common display devices. However, it is also important to focus on OLED displays, which constitute the next-generation displays already being mass produced by some manufacturers. The FETs for OLED displays require higher performances than those of LCDs, as they are driven by current.

Although large-sized and medium-sized LCD TVs and monitors still use a-Si TFTs, they are unable to sustain the increasing RC loads associated with the higher pixel counts and refresh rates. This problem was addressed by increasing the circuit scale and/or using division driving or other methods. However, this increased the cost and power consumption. Therefore, a-Si TFTs in these devices should be replaced by oxide semiconductor FETs. The currently mass-produced OLED TVs also use oxide semiconductor FETs because of their good current uniformity and compatibility with large-sized manufacturing.

LTPS TFTs are unsatisfactory for use in small displays with ultra-high pixel density. This will be discussed in detail later in this volume. They also face a challenge in the mass production of large displays.

This volume explains the reasons why CAAC-IGZO FETs can be applied to a wide range of displays (from large TVs to small displays with high pixel densities), as well as to circuit technologies of the displays using them. It also describes a fabrication technology for small and large foldable displays and the development of an apparatus for this purpose.

1.3 Transistor Technology for Displays

Various devices using flat-panel displays, such as TVs and smartphones, are widespread and indispensable in our daily life. The current mainstream flat-panel displays are LCDs. As next-generation displays, OLED displays are actively being developed by an increasing number of organizations [8]. Traditionally, hydrogenated amorphous silicon (a-Si:H) TFTs were widely employed for LCD TVs and monitors as switching elements.

As the demand for higher-performance display panels increases, FETs (in the following description, there are cases where the term “FETs” includes “TFTs”) with higher driving capability are required. This has led to the development of LTPS by several manufacturers [9–12]. However, since LTPS is fabricated by crystallizing a-Si, expertise is required to control the crystallization process. Furthermore, the application of LTPS to larger substrates is considered to be difficult compared with a-Si:H.

Recently, the use of oxide semiconductors as FETs has drawn much attention [13]. As mentioned in this book series, this class of semiconductor materials is remarkably different from Si; they have driving capabilities lower than that of LTPS but higher than that of a-Si:H. Oxide semiconductors are also characterized by their applicability to large substrates and relaxed fabrication requirements, such as low process temperatures and easy etching. Unlike LTPS, they do not require laser annealing, which is expensive and difficult for large substrates.

Oxide semiconductors offer an advantage in the form of higher driving capabilities but formerly had a disadvantage in the instability of the film formation and device characteristics compared with a-Si:H. Yamazaki and co-workers discovered crystalline IGZO (i.e., CAAC-IGZO; for more details, see [1]). This has a small film-defect density, enabling the fabrication of FETs with a short channel length, and thereby extending their applicability to high-resolution displays. CAAC-IGZO provides unique characteristics, including extremely low off-state current, compared with the widely used Si. This will be described in detail later.

This section reports on the process and characteristics of CAAC-IGZO FETs for display applications compared with those of Si.

1.3.1 Comparison of Silicon and Oxide Semiconductors

This subsection compares a-Si:H, LTPS, and IGZO. In terms of the FET fabrication process, a-Si:H is the shortest and contains fewer steps, followed by CAAC-IGZO, and LTPS is the longest. It is critical to reduce the number of process steps and their complexity to maximize the manufacturing yield. LTPS has a more extensive process than those of a-Si:H and CAAC-IGZO, as it requires the linear-beam laser crystallization of Si, high-temperature annealing, and ion doping. LTPS also has the disadvantage of expensive plant and equipment investment, because it requires special apparatus and expensive ion doping. The linear-beam laser equipment is also difficult to fabricate, especially for a large substrate such as G8. In contrast, a-Si:H and CAAC-IGZO technologies do not need any special apparatus, and are thus easily applicable for large substrates.

Semiconductor Energy Laboratory Co., Ltd. (SEL) initiated the development of linear-beam laser equipment (Figure 1.2) [14–17]. This was undertaken by equipment manufacturers in a widespread manner and is now indispensable for LTPS crystallization. The linear-beam laser equipment was initially developed for element separation in the modularization of solar cells. After using the linear-beam laser equipment for LTPS, SEL then researched CAAC-IGZO, with its high uniformity and large substrate capability.

Figure 1.2 Linear-beam laser equipment developed by SEL. *Source*: Reproduced from [17]. Copyright (2014), with permission from Wiley

Table 1.1 Substrate size class and intended use of a-Si:H, LTPS, and IGZO

	Resolution	a-Si:H	LTPS	CAAC-IGZO
Large TV	Higher	Fair	Poor	Good
(60 inch or more)	Lower	Good	Poor	Good
Medium TV	Higher	Good	Poor	Good
(20–55 inch)	Lower	Good	Poor	Good
Small and medium panel for tablet computers	Higher (4K2K)	Fair	Good	Good
(up to 10 inch)	Medium (FHD)	Good	Good	Good
	Lower (HD)	Good	Good	Good
Small and medium panel for smartphones	Higher (4K2K)	Fair	Good	Good
(up to 6 inch)	Medium (FHD)	Fair	Good	Good
	Lower (HD)	Good	Good	Good

Increasing the substrate size significantly contributed to lowering unit fabrication costs, as a larger substrate could yield a larger number of display panels. Table 1.1 lists some classes of substrate size intended for use in display manufacturing, and the potential for achieving high-resolution displays by employing silicon and oxide semiconductors. As described above, a-Si:H and CAAC-IGZO do not need any special equipment; thus, they could readily be applied to large substrates up to the tenth generation mother-glass size (approximately 3 m square). This allows the manufacture of large-sized TVs mainly by using LCD backplanes fabricated from a-S:H TFTs. Recent advances in the development of CAAC-IGZO have demonstrated that it also enables large TV fabrication. Additionally, it exhibits higher FET performance compared with a-Si:H, thereby enabling gate driver integration even for large TVs with high resolutions.

Large mother glasses also enable the manufacture of small-sized and medium-sized display panels in large volumes for smartphones and tablet computers. High resolution is a key factor for such panels, and requires increasing the FET driving capability. To date, LTPS with higher FET performance compared with a-Si:H was used for small and medium panels with high resolutions. Nevertheless, some aspects of the performance of CAAC-IGZO FETs are comparable with that of LTPS TFTs for small-sized and medium-sized panels. Therefore, CAAC-IGZO could be regarded as a prospective material for the production of display panels in a wide range of sizes and for various uses.

Figure 1.3 shows the FET characteristics of silicon and oxide semiconductors. FETs with silicon as an active layer exhibit a high off-state current, whereas the CAAC-IGZO FET exhibits an off-state current lower than the detection limit of the measurement apparatus. The low power consumption is an important characteristic for Displays. Applications utilizing the low off-state current will be described in Chapter 6 and elsewhere.

Table 1.2 compares silicon and oxide semiconductors in terms of manufacturability. Liquid crystal panels could be fabricated with almost the same number of masks as that of a-Si:H by using CAAC-IGZO [18, 19]. As the FET performance of CAAC-IGZO is higher than that of a-Si:H, it permits the narrowing of the bezels by integrating the gate driver on the panel (GOP), even in high-resolution displays [20]. The CAAC-IGZO FETs have an off-state current on the order of yoctoamps per micrometer (yA/μm) (where $y = 10^{-24}$) compared with femtoamps per micrometer (fA/μm) (where $f = 10^{-15}$) for LTPS TFTs and a-Si:H TFTs. As a result, it enables low-frequency display refresh and an associated lower power consumption (the panel driving power is proportional to the refresh frequency). This feature is also known as idling-stop (IDS) driving. IDS driving is a method for reducing power consumption for displays by showing

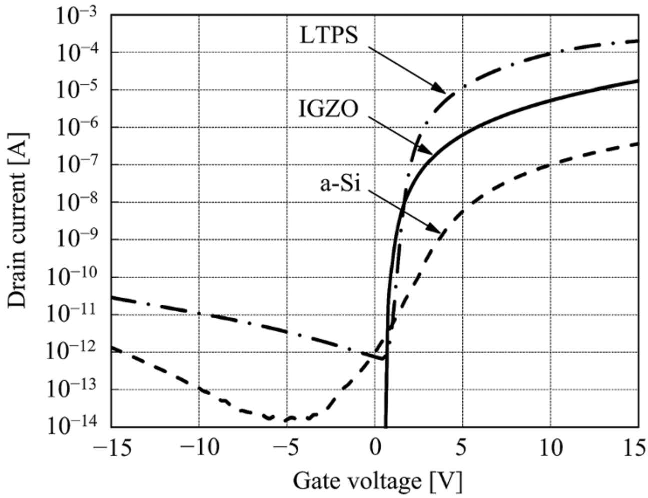


Figure 1.3 FET characteristics with an active layer of each semiconductor

Table 1.2 Comparison of a-Si:H, LTPS, and CAAC-IGZO. *Source*: Reprinted from [18, 19]. Copyright (2015), with permission from Wiley

	a-Si:H	LTPS	CAAC-IGZO
Number of masks for fabricating LCD (for FET only)	5–8 (4)	8–12 (5)	6–8 (4)
Process temperatures	350 °C	400 °C	350 °C
Gate driver	Depends on specifications	Applicable	Applicable
Mobility	Up to 1 cm^2/V-s	Up to 100 cm^2/V-s	Up to 40 cm^2/V-s
Size of mother glass	G4.5–G10	G4.5–G6	G4.5–G10
Device costs	Low	High	Low
Plant costs	Low	High	Low

static images. This topic will be described in detail in Chapter 6. IDS driving provides a significant power advantage, particularly for always-on, reflective or transflective mobile displays.

1.3.2 FETs in LCDs

FETs are used in pixel circuits, gate drivers, and other parts of LCDs and OLED displays. The characteristics of FETs required for these devices are briefly described below.

Figure 1.4 shows a pixel circuit of LCDs. The FET in the pixel circuit is used as a switch, as described in Figure 1.5. It performs image writing and retention operations when it is turned on and off, respectively.

As shown in the timing diagram illustrated in Figure 1.6, the retention operation is executed by turning off the pixel FET so that the voltage written into the capacitor Cs remains until the subsequent write period. As mentioned, IGZO features an extremely low off-state current that

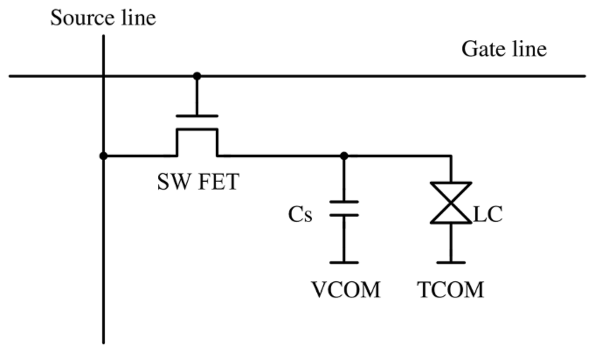


Figure 1.4 Circuit diagram of the LCD pixel

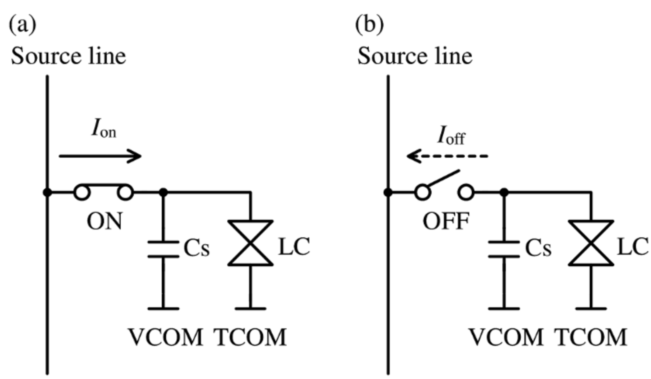


Figure 1.5 Circuit operation of LCD pixel: (a) writing operation; (b) retention operation

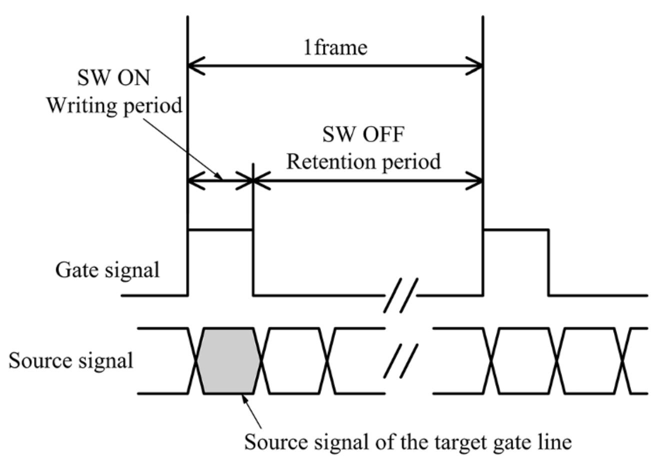


Figure 1.6 Timing diagram of gate and source signals used in the LCD pixel circuit

Table 1.3 Pixel capacitances and off-state current (allowable range of voltage shift is 20 mV)

	Required off-state current	
Capacitance per pixel	Standard driving (60 Hz)	IDS driving (1 Hz)
150 fF	1.8×10^{-13} A	3.0×10^{-15} A
15 fF	1.8×10^{-14} A	3.0×10^{-16} A

enables driving at a low refresh frequency. Table 1.3 shows the off-state current required for this type of driving. The maximum allowed off-state current depends on the storage capacitance of the pixel, and it has to be lower as the storage capacitance becomes smaller. As the resolution increases, the pixel size decreases, and hence the storage capacitor becomes small. Thus, a much lower off-state current is required for the IDS driving of high-resolution displays. In addition, the retention period is much longer than the writing period, thus, reliability is required in the off state, in which a negative voltage is applied to the gate.

The calculation conditions are as follows:

- Standard driving (60 Hz refresh rate)

$$I_{\mathrm{off}} = 150 \times 10^{-15} \times 0.02/\left(16.67 \times 10^{-3}\right) = 1.80 \times 10^{-13}\ \mathrm{A}.$$

- IDS driving (1 fps)

$$I_{\mathrm{off}} = 150 \times 10^{-15} \times 0.02/1 = 3 \times 10^{-15}\ \mathrm{A}.$$

Next, the image data-writing operation is described. The pixel FET is turned on to write image data to a pixel. A data voltage from a source line is written to the pixel capacitor Cs. In this case, the writing of the data voltage should be completed within the writing period, as shown in Figure 1.6.

If the on-state current is sufficiently large, the time constant of the source line, which is determined by a wiring resistance and parasitic capacitance, is generally larger than that of the pixel, which is determined by the on-state resistance of the switch FET and the storage capacitance. In the case of CAAC-IGZO FET or LTPS TFT, unlike a-Si, the channel width of the switch FET is determined by the design rule, and hence a large variety of LCDs can be driven.

Furthermore, as illustrated in Figure 1.7, the FETs function as a switch in the driver circuits. Figure 1.7 shows an output part in a driver circuit. The on-state current of the FET determines the time delay of the output part in a driver circuit, as shown in Figure 1.8. Therefore, a high on-state current is required for high-frequency operations in a driver circuit. In addition, a FET with large on-state current is necessary because the gate line has a large load capacitance. A method to increase the on-state current involves increasing the FET channel width. However, this also increases the driver circuit size, and thus the display bezel width.

As shown in Figures 1.7 and 1.8, a low off-state current is not as necessary in a driving circuit as in a pixel circuit. Nevertheless, the total power consumption of the driving circuit can be kept low by keeping this current as low as possible.

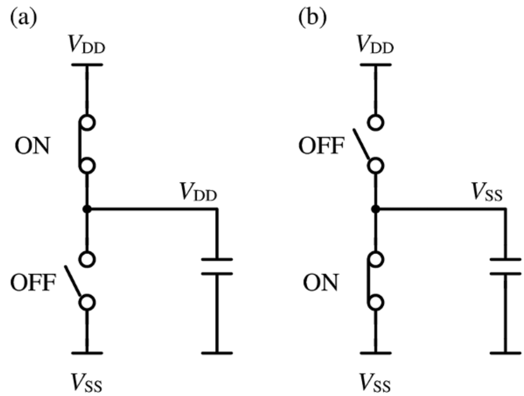


Figure 1.7 Examples of an output part in a driver circuit: (a) high output; (b) low output

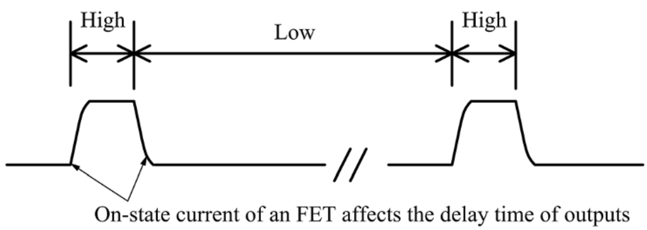


Figure 1.8 Waveform of an output from a driver circuit

1.3.3 FETs in OLED Displays

OLED displays consist of an array of self-emitting organic electroluminescent (EL) elements. Hence, unlike LCDs, they do not require any backlight source. Additionally, OLED displays could easily be made flexible. This is because the image formation is not based on optical retardation, a mechanism readily affected by even nanometer-sized changes in the display structure [21].

As shown in Figure 1.9, the OLED pixel luminance is proportional to the current per pixel. Thus, the image and display total dimming could easily be controlled. Conversely, the electro-optical transfer function of LCDs has an S-shape; thus, a look-up table (LUT) is necessary to achieve a linear response.

Driver circuits on a FET substrate for both OLED displays and LCDs comprise shift registers for selecting pixel rows. Thus, although the supply voltage is different, the *scan* or *gate*-driver circuits are almost identical. As shown in Figure 1.10, the pixel FET in an LCD functions as a *voltage* switch. In contrast, the driving FET in an OLED pixel adjusts the *current* flowing through the OLED element, which is connected serially with the driving FET (M2) [18]. This indicates that the OLED luminance also changes by degradations in the OLED element and/or driving FET, resulting in an undesired variation in the luminance across the panel. Therefore, OLED displays generally contain compensation circuits that keep the current constant by adjusting the driving voltage. However, as the degradation progresses, there is a voltage limit by which this compensation could be carried out.

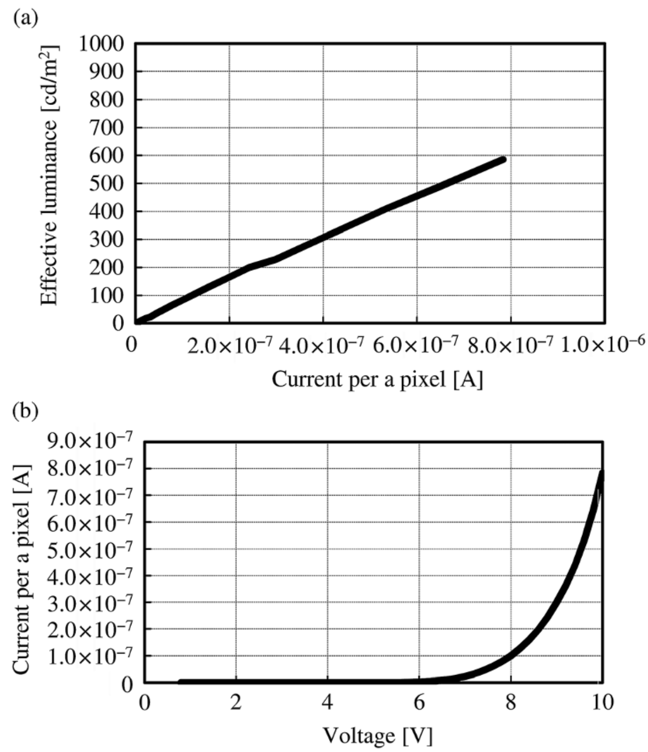


Figure 1.9 Current–effective luminance characteristics of the OLED element and voltage–current characteristics (blue element)

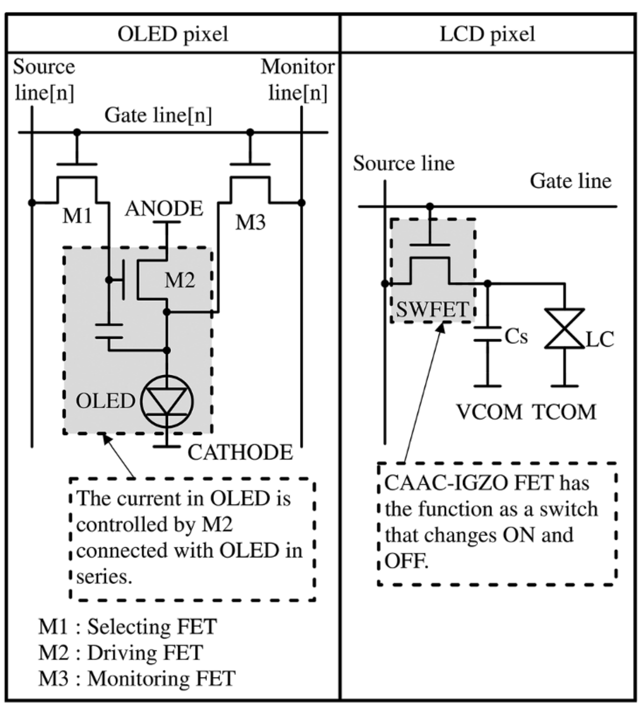


Figure 1.10 Examples of the pixel circuit configurations of OLED display (left) and LCD (right)

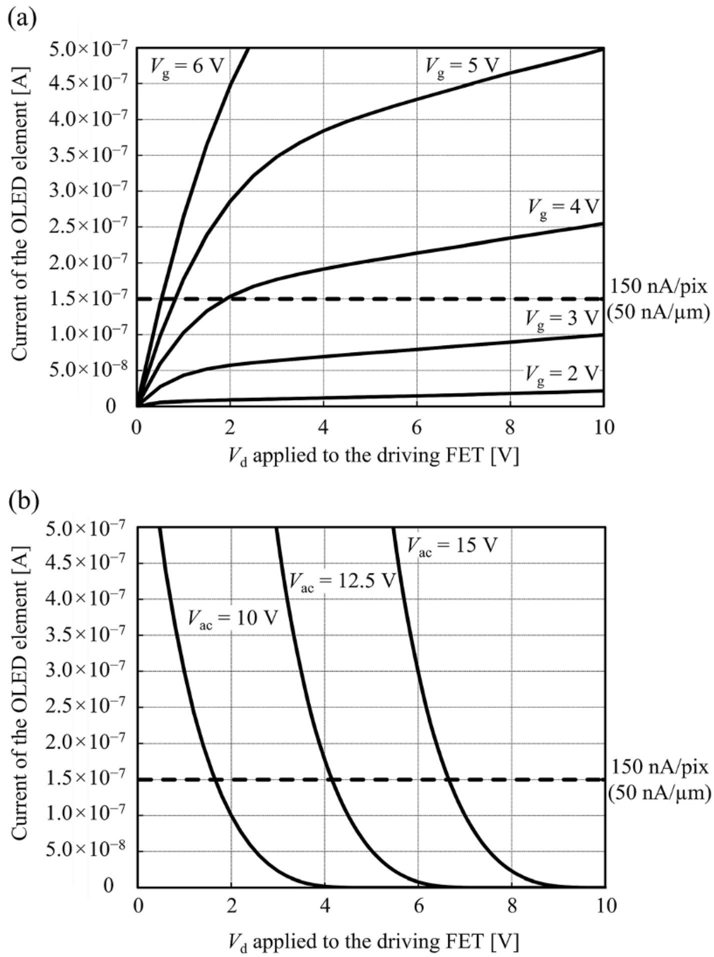


Figure 1.11 I_d–V_d characteristics of the driving FET (a) and *I*–*V* characteristics of the OLED element (b). FET characteristics: $L/W = 6/3$ μm, EL characteristics: blue element

V_d can be expressed by as follows:

$$V_d = V_{ac} - V_{el}, \tag{1.1}$$

where

V_d = voltage between the source and drain of the driving FET
V_{el} = voltage drop across the OLED element
V_{ac} = voltage between the OLED cathode and the drain of the driving FET.

Therefore, V_d of the driving circuit is adjusted according to the changes in OLED element resistance associated with its degradation.

As shown in Figure 1.11, the light emission from the OLED element in an OLED display depends on the *I–V* characteristics of both the driving FET and OLED elements. The intersection between the two *I–V* curves gives the current value for light emission. The OLED element emits light proportional to the current value.

Accordingly, the current flowing through the driving transistor (and OLED element) decreases as a result of degradation [downward shift in Figure 1.11(a)], that is, a shift in V_d. Furthermore, the luminance and anode/cathode voltage is reduced accordingly, as indicated by a leftward shift in Figure 1.11(b).

It is important to use the anode/cathode voltage in the *I–V* saturation region of the driving FET to minimize the influence of V_d reduction by degradation of the OLED element. Therefore, the saturation characteristics (current independent of the voltage) of the driving FET are important.

From the above discussion, the following three features of driving FETs are considered necessary.

1. Constant current characteristics (saturation in I_d–V_d characteristics).
2. Reduction in spatial current variation (especially variation between adjacent pixel FETs).
3. Stability over time (such as drain current variation resulting from current stress).

1.3.4 Recent FET Technologies

LCD and OLED display backplanes with various CAAC IGZO materials and FET structures were developed and evaluated to obtain the three previously discussed features. Figures 1.12–1.14 show comparisons of the *I–V* characteristics, on-state currents, *S*-values of several types of CAAC-IGZO, and commercialized LTPS TFTs. The CAAC-IGZO FETs have a top-gate self-aligned (TGSA) structure, which will be introduced in Section 2.3. It should be noted that "nIGZO" and "sIGZO" in the figures are new materials, which will be described in detail in Section 2.4: nIGZO is a high-mobility CAAC-IGZO and sIGZO is a material that exhibits further higher mobility than nIGZO [22].

Even with a channel length of $L = 2$ μm, the sIGZO FET exhibits improved on-state current (the field-effect electron mobility was approximately 60 cm^2/V-s). This was equivalent to the mobility of the commercialized LTPS TFT ($L \approx 6.4$ μm). Simultaneously, the sIGZO FET maintained the normally-off characteristics of nIGZO. The *S*-value of the sIGZO FET was approximately half that of the LTPS TFT. This indicated that it was more suitable for low-voltage driving compared with LTPS TFTs.

Figure 1.15 shows the results of gate bias temperature (GBT) stress tests. As shown, the change in threshold voltage as a result of the stress was similar for the sIGZO FET and the *p*-channel LTPS TFT in a gate driver. Details of the GBT stress test will be given in Section 2.5.

As previously mentioned, the two FET requirements for OLED display driving include the following: (1) a constant current irrespective of the changes in the drain voltage V_d; (2) a small current change from FET deterioration. As shown in Figure 1.16, the $I_d - V_d$ saturation characteristics of FETs used for driving the OLEDs were measured to evaluate both the aforementioned factors; the saturation properties of the LTPS TFT are not enough, even with a channel length of $L \approx 6.4$ μm [23]. This was attributed to a short-channel effect, and suggested that there was a limitation on scaling down the LTPS TFT size. However, the nIGZO

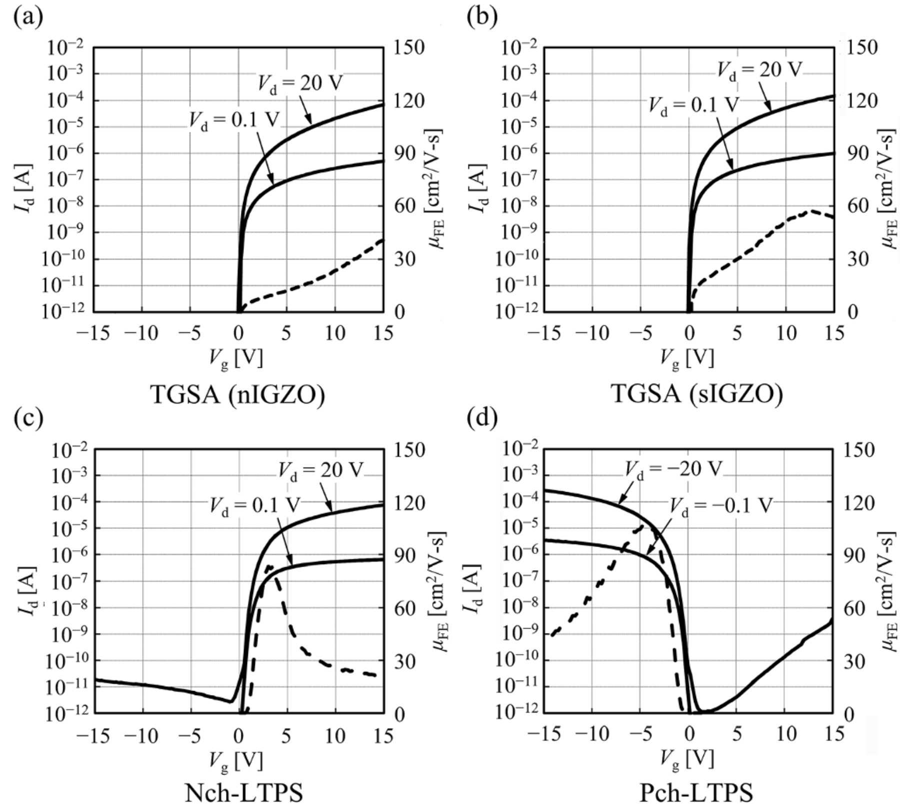
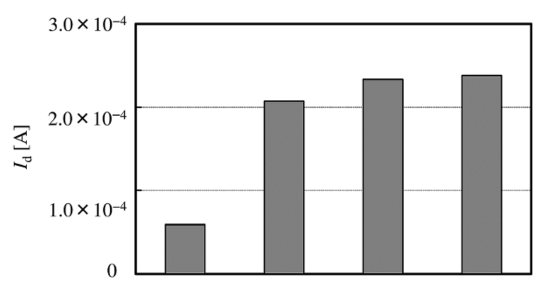


Figure 1.12 I_d–V_g characteristics of FETs with different semiconductor configurations. Measurement conditions: $V_g = -15$ to 15 V (0.25 V step), $V_d = 0.1$, 20 V, and $V_s = 0$ V (COMMON). Solid and dashed lines denote I_d–V_g and mobility (at $V_d = 20$ V) curves, respectively. The channel lengths (L) and widths (W) are (a) $L/W = 2/3$ μm, (b) $L/W = 2/3$ μm, (c) $L/W = 2.7 \times 2/3$ μm, and (d) $L/W = 3.2 \times 2/6.4$ μm. LTPS has two gates aligned parallel in the same plane, connected in series, each with a length of 2.7 μm in (c) and 3.2 μm in (d)



nIGZO	sIGZO	Nch	Pch
TGSA Structure		Commercialized LTPS	
$L/W = 2/20$ μm		$L/W = 3.2 \times 2/18.9$ μm	

Figure 1.13 Comparison of the on-state current between FETs with different semiconductor layers ($|V_g| = 10$ V and $|V_d| = 5$ V)

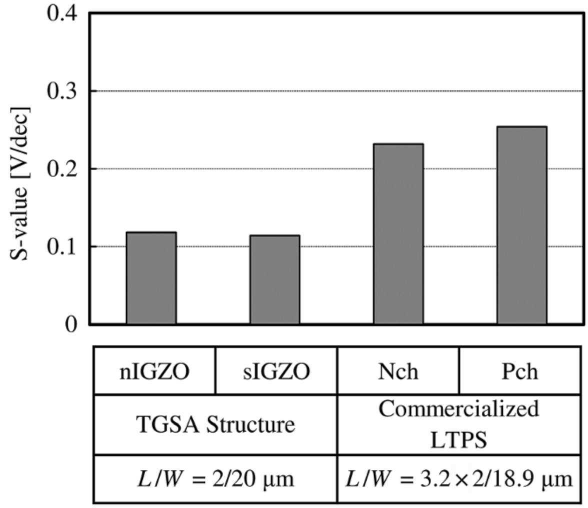


Figure 1.14 Comparison of S-values between FETs with different semiconductor layers ($|V_d| = 10$ V)

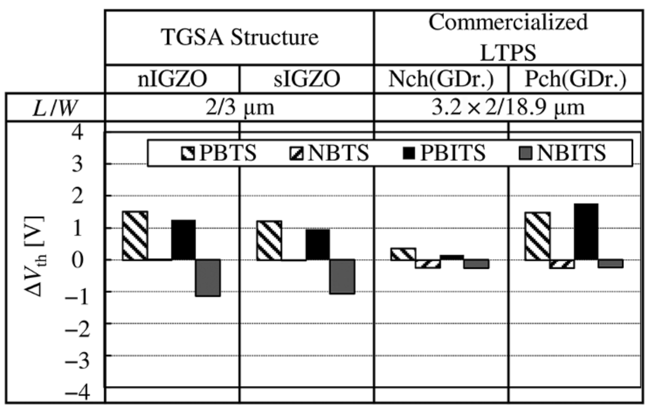


Figure 1.15 Results of the GBT stress tests of FETs with different semiconductor materials and structures. Test conditions: $V_g = \pm 30$ V and $V_d = V_s = 0$ V (COMMON); stress temperature 60 °C; application time of stress 1 h; dark/photo stress (pseudo-white OLED, 10,000 lx). PBTS, NBTS, PBITS, and NBITS stand for positive bias temperature stress, negative bias temperature stress, positive bias illumination temperature stress, and negative bias illumination temperature stress, respectively

and sIGZO FETs exhibited sufficient saturation even with a short channel length of $L = 2$ μm. This proved that CAAC-IGZO FETs are highly resistant to the short-channel effect, and thereby enabled FET size reduction. It also resulted in higher display resolutions and smaller footprints.

Lastly, the FET characteristic of the latest IGZO is presented in Figure 1.17. The latest IGZO has a mobility of a record of 100 cm^2/V-s or higher. Thus, in the near future, IGZO is expected to achieve a practical level with higher mobility than LTPS.

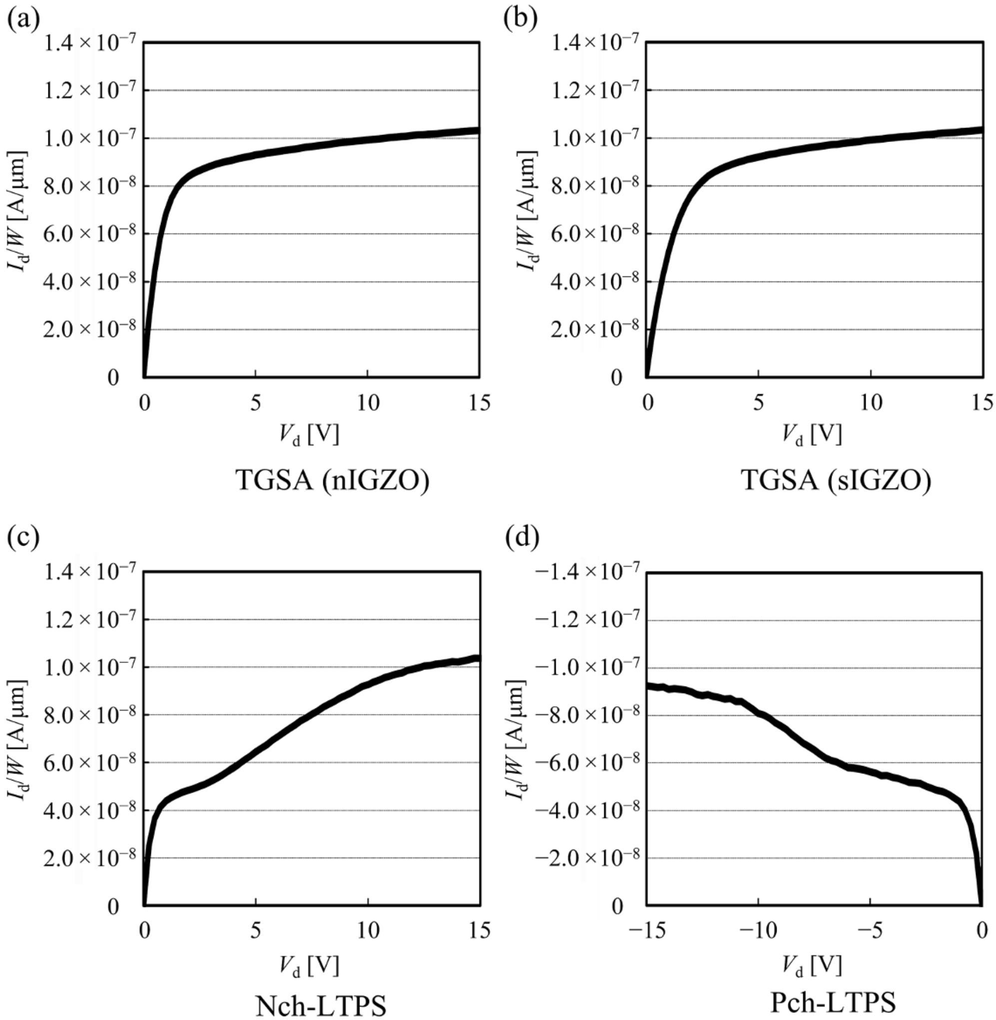


Figure 1.16 Comparison of the saturation characteristics of FETs with different semiconductor materials and structures. Measurement conditions: $I_d - V_d$: $V_d = 0$ to 15 V (0.25 V step); V_g is a voltage at which $I_d/\mathrm{W} = 100$ nA/μm at $|V_d| = 10$ V; $V_s =$ GND; room temperature; dark environment. The channel lengths (L) and widths (W) are as follows: (a, b): $L/W = 3/3$ μm, (c, d): $L/W = 3.2 \times 2/6.4$ μm. *Source*: Adapted from [23]. Reprinted with permission of Wiley

1.3.5 Development of OLED Displays

As described in the previous sections, CAAC-IGZO FETs have several advantages over Si TFTs. Therefore, displays are developed with CAAC-IGZO FETs to exploit these advantages. In particular, CAAC-IGZO matches the requirements of ultra-high-resolution OLED displays and flexible OLED displays for wearable devices. The details of these devices will be described in the following chapters. Figure 1.18 illustrates the current development status of the OLED

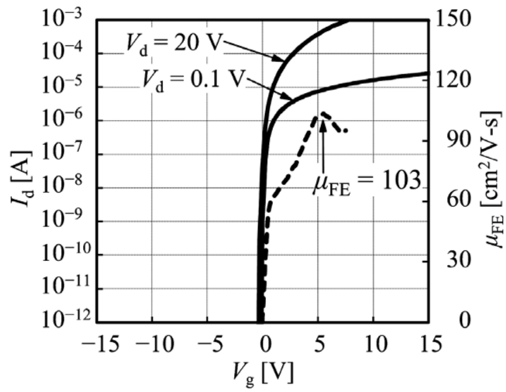


Figure 1.17 I_d–V_g characteristics of FETs with the latest IGZO

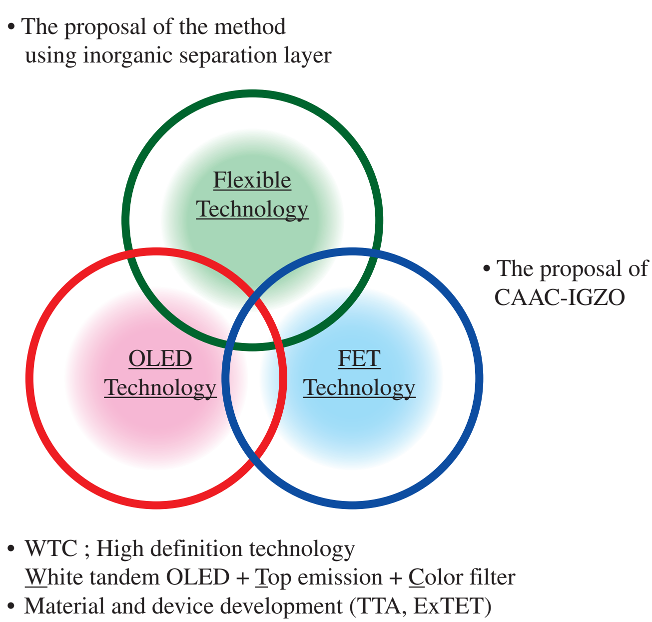


Figure 1.18 The developments for OLED displays

displays. The development of the OLED materials and FETs for a transfer process (see Chapter 5) to enable flexible display fabrication is currently in progress. As shown in Figure 1.19, the display resolution has increased steadily since 2012. This was also reported at various exhibitions and academic societies, including the Society for Information Display (SID) [24–28]. This volume offers an in-depth discussion of the fabrication of OLED displays reported at SID and elsewhere. The authors hope that the reader will find this information useful (see Chapters 4 and 5).

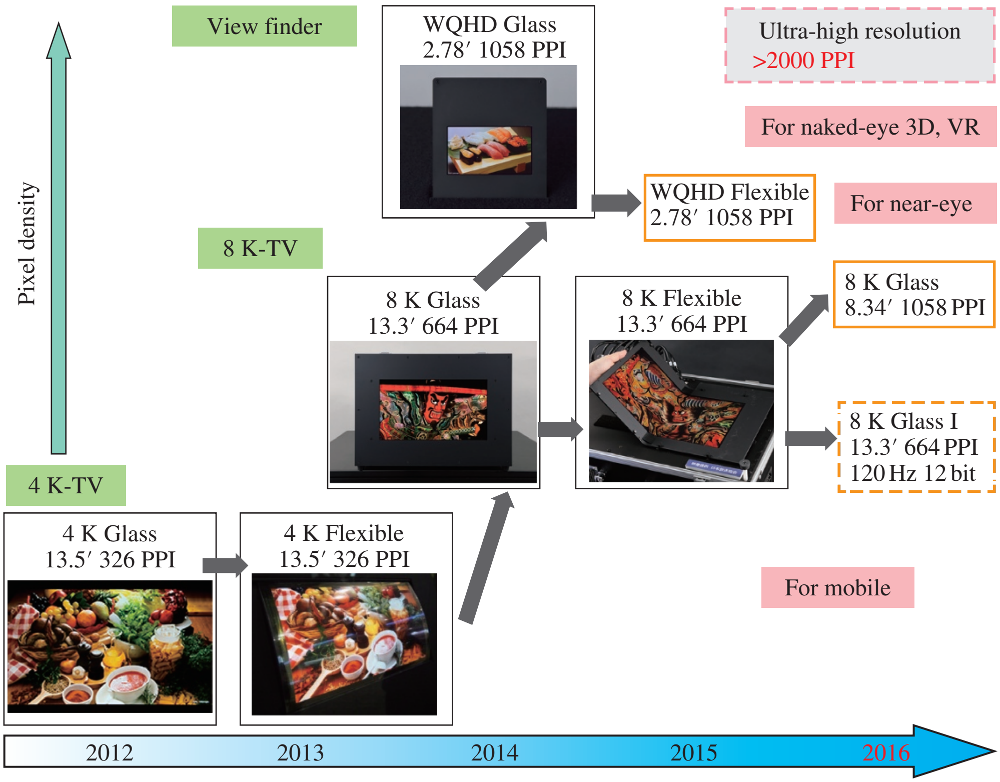


Figure 1.19 The transition timeline of the developments in OLED displays

Subsequent chapters explain the two types of CAAC-IGZO FET structure and their fabrication processes. This is followed by descriptions of the circuit designs for displays using CAAC-IGZO.

References

[1] Yamazaki, S. and Kimizuka, N. (in press) *Physics and Technology of Crystalline Oxide Semiconductor CAAC-IGZO: Fundamentals*. Chichester, UK: John Wiley.

[2] Yamazaki, S. and Fujita, M. (in press) *Physics and Technology of Crystalline Oxide Semiconductor CAAC-IGZO: Application to LSI*. Chichester, UK: John Wiley.

[3] Ukai, Y. (2007) *Thin Film Transistor*. Tokyo: Kogyo Chosakai Publishing [in Japanese].

[4] Lechner, B. J., Marlowe, F. J., Nester, E. O., and Tults, J. (1971) "Liquid crystal matrix displays," *Proc. IEEE*, **59**, 1566. http://dx.doi.org/10.1109/PROC.1971.8489

[5] Shishikui, Y. (2013) Research and Development of Super Hi-Vision. NHK Science & Technology Research Laboratories (STRL) R&D No. 137. Available at: www.nhk.or.jp/strl/publica/rd/rd137/PDF/P04-09.pdf [in Japanese].

[6] Sugawara, M. (2008) "Super hi-vision research on a future ultra-HDTV system," *EBU Tech. Rev*. Available at: tech.ebu.ch/docs/techreview/trev_2008-Q2_nhk-ultra-hd.pdf.

[7] le Comber, P. G., Spear, W. E., and Ghaith, A. (1979) "Amorphous-silicon field-effect device and possible application," *Electron. Lett.*, **15**, 179. http://dx.doi.org/10.1049%2Fel%3A19790126

[8] Tsujimura, T. (2012) *OLED Display Fundamentals and Applications*. Chichester, UK: John Wiley.

[9] Oana, Y., Kotake, H., Mukai, N., and Ide, K. (1983) "Electrical properties of polycrystalline-silicon MOSFETs on glass," *Jpn. J. Appl. Phys.*, **22**(22-1), 493. http://dx.doi.org/10.7567/JJAPS.22S1.493

[10] Morozumi, S. (1989) "Poly-Si TFTs for large-area applications," *Japan Display.*, **89**, 148.

[11] Sameshima, T., Usui, S., and Sekiya, M. (1986) "XeCl excimer laser annealing used in the fabrication of poly-Si TFTs," *IEEE Electron Device Lett.*, **7**, 276. http://dx.doi.org/10.1109/EDL.1986.26372

[12] Serikawa, T., Shirai, S., Okamoto, A., and Suyama, S. (1989) "Low-temperature fabrication of high-mobility poly-Si TFTs for large-area LCDs," *IEEE Trans. Electron Devices*, **36**, 1929. http://dx.doi.org/10.1109/16.34272

[13] Yamazaki, S., Hirohashi, T., Takahashi, M., Adachi, S., Tsubuku, M., Koezuka, J., *et al.* (2014) "Back-channel-etched thin-film transistor using *c*-axis-aligned crystal In–Ga–Zn oxide," *J. Soc. Inf. Disp.*, **22**, 55. http://dx.doi.org/10.1002/jsid.211

[14] Yamazaki, S., Zhang, H., and Ishihara, H. (1999) US Patent 6,002,101.

[15] Shinohara, H. and Sugawara, A. (1998) US Patent 6,149,988.

[16] Kubo, N., Kusumoto, N., Inushima, T., and Yamazaki, S. (1994) "Characteristics of polycrystalline-Si thin film transistors fabricated by excimer laser annealing method," *IEEE Trans. Electron Devices*, **41**, 1876. http://dx.doi.org/10.1109/16.324604

[17] Yamazaki, S. (2014) "Future possibility of c-axis-aligned crystalline oxide semiconductor: Comparison with low-temperature polysilicon," *SID Symp. Dig. Tech. Pap.*, **45**, 9. http://dx.doi.org/10.1002/j.2168-0159.2014.tb00003.x

[18] Takahashi, K., Sato, T., Yamamoto, R., Shishido, H., Isa, T., Eguchi, S., *et al.* (2015) "13.3-inch 8k4k 664-ppi foldable OLED display using crystalline oxide semiconductor FETs," *SID Symp. Dig. Tech. Pap.*, **46**, 250. http://dx.doi.org/10.1002/sdtp.10453

[19] Shima, Y., Kanemura, H., Higano, S., Hosaka, Y., Okazaki, K., Koezuka, J., *et al.* (2015) "Channel-etched CAAC-OS FETs using multi-layer IGZO," *SID Symp. Dig. Tech. Pap.*, **46**, 1158. http://dx.doi.org/10.1002/sdtp.10037

[20] Toyotaka, K., Miyake, H., Kaneyasu, M., Yamashita, A., Jikumaru, M., Koyama, J., *et al.* (2014) "513-ppi liquid crystal display using c-axis aligned crystalline oxide semiconductor with narrow bezel and aperture ratio greater than 50%," *SID Symp. Dig. Tech. Pap.*, **45**, 634. http://dx.doi.org/10.1002/j.2168-0159.2014.tb00166.x

[21] Hatano, K., Chida, A., Okano, T., Sugisawa, N., Inoue, T., Seo, S., *et al.* (2010) "3.4-inch QHD flexible AMOLED with oxide TFT," *Proc. AM-FPD'10 Dig.*, 263.

[22] Okazaki, K., Kanemura, H., Kurosaki, D., Shima, Y., Koezuka, J., Kawashima, S., *et al.* (2015) "Fabrication of 8k4k organic EL panel using high-mobility IGZO material," *SID Symp. Dig. Tech. Pap.*, **46**, 939. http://dx.doi.org/10.1002/sdtp.10415

[23] Shima, Y., Jincho, M., Hamochi, T., Saito, S., Dobashi, M., Okazaki, K., *et al.* (2016) "Development of a top-gate transistor with short channel length and c-axis-aligned crystalline indium–gallium–zinc-oxide for high-resolution panels," *SID Symp. Dig. Tech. Pap.*, **47**, 1037. http://dx.doi.org/10.1002/sdtp.10920

[24] Tanabe, T., Amano, S., Miyake, H., Suzuki, A., Komatsu, R., Koyama, J., *et al.* (2012) "New threshold voltage compensation pixel circuits in 13.5-inch Quad full high definition OLED display of crystalline In–Ga–Zn-oxide FETs," *SID Symp. Dig. Tech. Pap.*, **43**, 88. http://dx.doi.org/10.1002/j.2168-0159.2012.tb05717.x

[25] Eguchi, S., Shinoda, H., Isa, T., Miyake, H., Kawashima, S., Takahashi, M., *et al.* (2012) "13.5-inch Quad-FHD top-emission OLED display using crystalline-OS-FET," *SID Symp. Dig. Tech. Pap.*, **43**, 367. http://dx.doi.org/10.1002/j.2168-0159.2012.tb05792.x

[26] Aoyama, T., Komatsu, R., Nakazato, R., Ohno, N., Jinbo, Y., Eguchi, S., *et al.* (2013) "13.5-inch Quadra-FHD flexible AMOLED with crystalline oxide FET," *Proc. AM-FPD'13 Dig.*, 223.

[27] Kawashima, S., Inoue, S., Shiokawa, M., Suzuki, A., Eguchi, S., Hirakata, Y., *et al.* (2014) "13.3-in. 8 K × 4 K 664-ppi OLED display using CAAC-OS FETs," *SID Symp. Dig. Tech. Pap.*, **45**, 627. http://dx.doi.org/10.1002/j.2168-0159.2014.tb00164.x

[28] Yokoyama, K., Hirasa, S., Miyairi, N., Jimbo, Y., Toyotaka, K., Kaneyasu, M., *et al.* (2015) "A 2.78-in 1058-ppi ultra-high-resolution OLED display using CAAC-OS FETs," *SID Symp. Dig. Tech. Pap.*, **46**, 1039. http://dx.doi.org/10.1002/sdtp.10376

2

Applications of CAAC-IGZO FETs to Displays

2.1 Introduction

As described in Chapter 1, a field-effect transistor (FET) using *c*-axis-aligned crystalline indium–gallium–zinc oxide (CAAC-IGZO) offers advantages over thin-film transistors (TFTs) based on hydrogenated amorphous silicon (a-Si:H) or low-temperature polysilicon (LTPS). For instance, one advantage of using CAAC-IGZO as a backplane of a liquid crystal display (LCD) panel is the possibility of slow-refresh driving (see Chapter 6), which exploits the extremely low off-state current of the FETs. Another advantage is that the FET size can be reduced to increase the aperture ratio, while retaining the high mobility, and demultiplexers (DEMUX) as well as gate drivers can be incorporated to achieve a bezel width equivalent to that of an LTPS display. Finally, CAAC-IGZO panels can be manufactured with equipment and running cost comparable to those of a-Si:H, and existing manufacture lines can be used. Because of these advantages, CAAC-IGZO FETs are being employed in backplanes for flat-panel displays. Furthermore, the FETs also find applications in low-power large-scale integration (LSI) devices such as central processing units (CPUs) and memories, as described in detail in *Physics and Technology of Crystalline Oxide Semiconductor CAAC-IGZO: Applications to LSI* [1].

Although the CAAC-IGZO active layers are formed by film-deposition process, the structures of the FETs are sometimes beyond the category of TFTs (e.g., like those used in LSI applications). Therefore, the term "CAAC-IGZO FET" is used in this book, instead of "CAAC-IGZO TFT." As is generally known, the metal–oxide–semiconductor field-effect transistors (MOSFETs) mainly used in displays are often called "TFTs," and in some cases the "CAAC-IGZO FETs" shown in this book can be regarded as "CAAC-IGZO TFTs."

In this chapter, four structures of FETs for the backplane of LCDs and organic light-emitting diode (OLED) displays are explained. The FETs based on CAAC-IGZO as an active layer

---

Physics and Technology of Crystalline Oxide Semiconductor CAAC-IGZO: Application to Displays, First Edition.
Edited by Shunpei Yamazaki and Tetsuo Tsutsui.

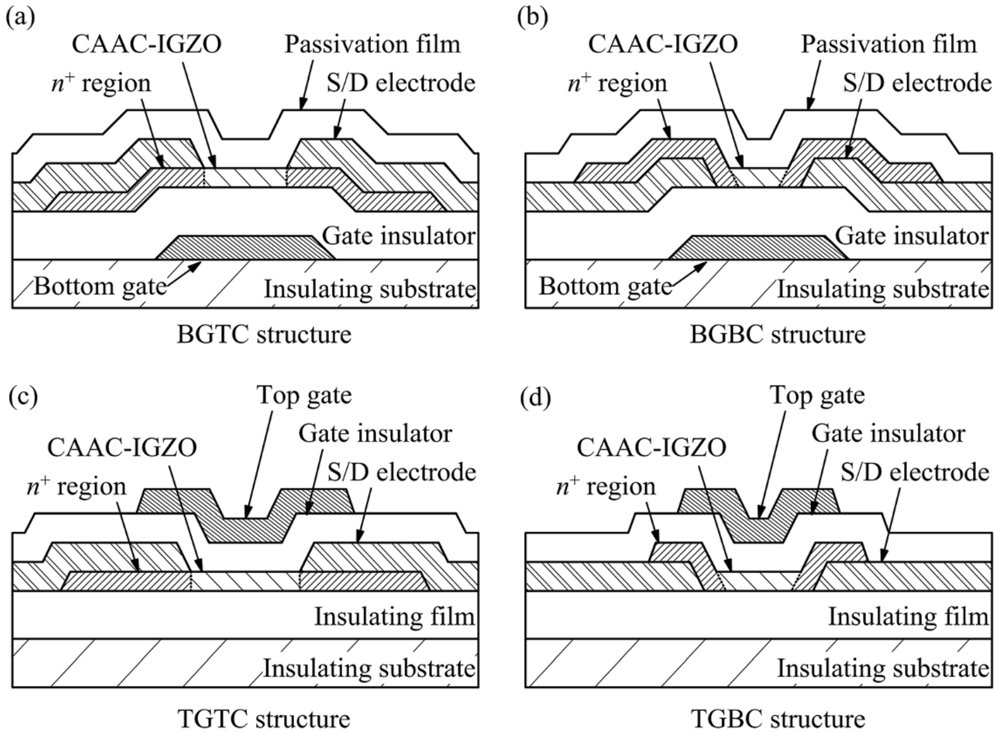


Figure 2.1 Examples of FET structures: (a) BGTC structure, (b) BGBC structure, (c) TGTC structure, (d) TGBC structure. *Source*: Adapted from [2]

belong to the category of MOSFETs, which control the current across the source/drain (S/D) regions, using a gate field through an insulating film. The FETs can be roughly classified into the following four structures, depending on the positions of the active layer, gate electrode (GE), and S/D electrodes (see Figure 2.1):

a. bottom-gate top-contact (BGTC)
b. bottom-gate bottom-contact (BGBC)
c. top-gate top-contact (TGTC)
d. top-gate bottom-contact (TGBC).

The position of the gate electrode determines the structure to be either top-gate or bottom-gate; the top-gate structure has a gate electrode above the CAAC-IGZO active layer, while it is located below it in the bottom-gate structure. Meanwhile, the position of the S/D electrodes determines whether the structure is top- or bottom-contact. In the former, the S/D electrodes are located above the active layer, whereas they are located below it in the latter. Thus, the combination of these structures determines FET structures (a)–(d).

Among the structures in Figure 2.1, bottom-contact structures [(b) BGBC and (d) TGBC] have the active layer sputtered on top of the S/D electrodes, so CAAC-IGZO is immune to any damage caused by S/D electrode formation (e.g., during deposition or etching). However, CAAC-IGZO is sputtered in an oxygen atmosphere and thus oxide films are formed on the

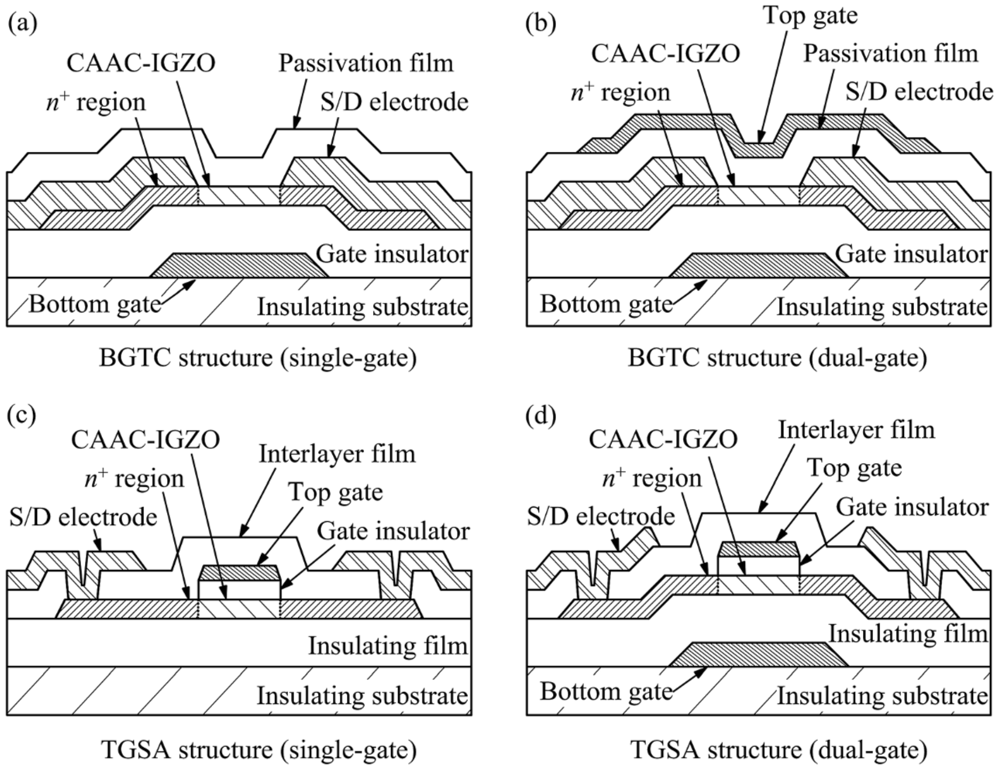


Figure 2.2 Examples of FET structures: (a) BGTC with a single gate, (b) BGTC with a dual gate, (c) TGSA with a single gate, (d) TGSA with a dual gate. *Source*: Adapted from [2]

surfaces of S/D electrodes, thereby increasing their contact resistance. The amount of oxide formation depends on the electrode materials.

Note that in addition to the four structures shown in Figure 2.1, other types of structure are possible, for example, a dual-gate structure, which has gate electrodes both on the top and bottom of the active layer [3], and a top-gate self-aligned (TGSA) structure, which has n^+ regions self-aligned to the gate-electrode pattern [4]. Figure 2.2 shows cross-sectional views of these structures.

BGTC and TGSA structures, described in Sections 2.2 and 2.3, respectively, are mainly developed for displays because the FET size and parasitic capacitance of the structures can be reduced. They can be used in all display sizes, from small- and medium-sized mobile high-resolution displays to large displays for 8K TVs. Sections 2.2 and 2.3 specifically describe the advantages and disadvantages, and explain the process flows and electrical characteristics of the two structures. Section 2.4 explains ways of maximizing the performance and reliability of CAAC-IGZO FETs by selecting high-mobility oxide semiconductor material and/or dual-gate structure with a surrounded-channel (S-channel). These technologies allow the fabrication of FETs with a performance and reliability equivalent to LTPS TFTs.

Section 2.5 explains how to counter the typical degradation mode of CAAC-IGZO FETs [i.e., degradation due to negative bias illumination temperature stress (NBITS)] and the mechanism that causes it. It also explains the main factors of NBITS degradation; deep level defects in the oxide semiconductor (oxide vacancies V_O) and defect levels in the gate insulator (GI)