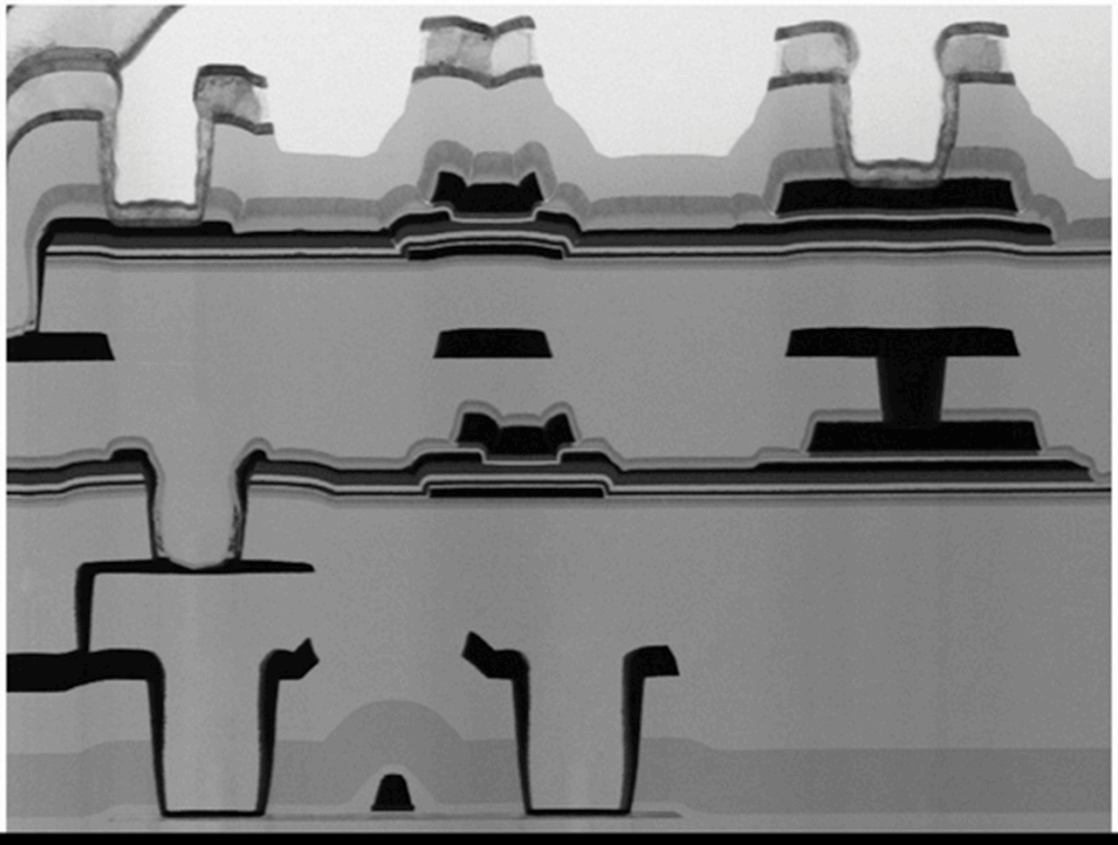
PHYSICS AND TECHNOLOGY OF CRYSTALLINE OXIDE SEMICONDUCTOR CAAC-IGZO

APPLICATION TO LSI

Edited by
Shunpei Yamazaki and Masahiro Fujita



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APPLICATION TO LSI

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WILEY

This edition first published 2017
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Library of Congress Cataloging-in-Publication Data

Names: Yamazaki, Shunpei, 1942– author. | Fujita, Masahiro, 1956– author.
Title: Physics and technology of crystalline oxide semiconductor CAAC-IGZO.
Application to LSI / Shunpei Yamazaki, Masahiro Fujita.
Description: Chichester, West Sussex, United Kingdom : John Wiley & Sons, Ltd
Registered office John Wiley & Sons Ltd, [2017] | Includes bibliographical references and index.
Identifiers: LCCN 2016025860 | ISBN 9781119247340 (cloth) | ISBN 9781119247432 (epub) |
ISBN 9781119247425 (Adobe PDF)
Subjects: LCSH: Semiconductors–Materials. | Semiconductors–Characterization. |
Gallium compounds. | Zinc compounds.
Classification: LCC TK7871.85 .Y357598 2016 | DDC 621.39/5–dc23
LC record available at https://lccn.loc.gov/2016025860

A catalogue record for this book is available from the British Library.

Set in 10/12pt Times by SPi Global, Pondicherry, India

10 9 8 7 6 5 4 3 2 1

Contents

About the Editors

Shunpei Yamazaki received his Ph.D., ME, BE, and honorary degrees from Doshisha University, Japan, in 1971, 1967, 1965, and 2011, respectively, and is the founder and president of Semiconductor Energy Laboratory Co., Ltd. He invented a basic device structure of non-volatile memory known as "flash memory" in 1970 during his Ph.D. program. Yamazaki is a distinguished foreign member of the Royal Swedish Academy of Engineering Sciences and a founder of Kato & Yamazaki Educational Foundation. Yamazaki has published or co-published over 400 papers and conference presentations and is the inventor or co-inventor of over 6314 patents (Guinness World Record in 2011).

1967	Completed Master's Degree Program at Doshisha University Graduate School of Engineering
1970	Invented a basic device of flash memory (Japanese Patent No. 886343; Japanese Examined Patent Application Publication No. Sho50-36955)
1971	Received Ph.D. in Engineering from Doshisha University Graduate School Doctoral Program Joined TDK Corporation (formerly TDK Electronics Co., Ltd.)
1980	Established Semiconductor Energy Laboratory Co., Ltd. and assumed position as president
1984	Awarded the Richard M. Fulrath Award by the American Ceramic Society (for research on MIS structure)
1995	Awarded the Medal with Dark Blue Ribbon from the Cabinet Office of the Japanese government (proceeds given to Japanese Red Cross Society) (awarded 6 times since 2015)
1997	Awarded the Medal with Purple Ribbon from the Cabinet Office of the Japanese government (for development of MOS LSI element technology)
2009	IVA (Royal Swedish Academy of Engineering Science) Foreign Member
2010	Awarded Okochi Memorial Technology Award from Okochi Memorial Foundation
2011	IEEE Life Fellow Received Honorary Doctor Degree of Culture from Doshisha University

Renewed his first Guinness World Record in 2004 (man holding the most patents in the world)
2015 Granted the title of "Friend of Doshisha" by Doshisha University
2015 SID Special Recognition Award for "discovering CAAC-IGZO semiconductors, leading their practical application, and paving the way to next-generation displays by developing new information-display devices such as foldable or 8K × 4K displays"

Masahiro Fujita received his Ph.D. in Information Engineering from the University of Tokyo in 1985 on his work on model checking of hardware designs by using logic programming languages. In 1985, he joined Fujitsu as a researcher and started to work on hardware automatic synthesis as well as formal verification methods and tools, including enhancements of BDD/SAT-based techniques. From 1993 to 2000, he was director at Fujitsu Laboratories of America and headed a hardware formal verification group which was developing a formal verifier for real-life designs having more than several millions of gates. The developed tool has been used in production internally at Fujitsu and externally as well. Since March 2000, he has been a professor at VLSI Design and Education Center in the University of Tokyo. He has done innovative works in the areas of hardware verification, synthesis, testing, and software verification mostly targeting embedded software and web-based programs. He has been involved in a Japanese governmental research project for dependable system designs and has developed a formal verifier for C programs that could be used for both hardware and embedded software designs. The tool is now under evaluation jointly with industry with governmental support. He has authored and co-authored 10 books, and has more than 300 publications and has been given several awards from scientific societies. He has been involved as program and steering committee members in many prestigious conferences on CAD, VLSI designs, software engineering, and more. His current research interests include synthesis and verification of SoC (System on Chip), hardware/software co-designs targeting embedded systems and cyber physical systems, digital/analog co-designs, and formal analysis, verification, and synthesis of embedded programs.

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Toshihiko Takeuchi	Semiconductor Energy Laboratory Co., Ltd.
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Naoaki Tsutsui	Semiconductor Energy Laboratory Co., Ltd.
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Series Editor's Foreword

The convergence of personal electronic devices towards small, powerful and multifunctional platforms throws into relief the conflict for resources between the display and other system electronics. On the one hand, high-quality, high-resolution and bright displays not only provide an essential human interface, but are one of the decisive factors in attracting users to purchase a device and differentiate between different models. On the other hand, the display has no purpose without the electronic systems which control and supply content to it – functions which now require powerful, fast data processing and information storage capabilities. Both display and system electronics must share the limited energy stored in a small, lightweight battery, and achieving excellent performance from the whole device, combined with adequate battery life from a small package, is a central challenge.

In this volume, Dr. Yamazaki and Professor Fujita bring together a comprehensive account of how CAAC oxide semiconductors can contribute to the ecosystem of large-scale integrated electronics. Many of the developments presented here provide routes to making major power-consumption savings in the operation of electronic systems. In other cases, performance improvements or new capabilities arise from the use of these CAAC oxide components: this is the case, for example, in the imaging sensors presented in Chapter 7 of this book.

The book you are holding is one of the three volumes planned by Dr. Yamazaki and his colleagues, to give a comprehensive overview of CAAC-IGZO technology. The first volume presents the basic science and technology of the materials: deposition conditions, structure, physical properties, and the physics and performance of the semiconductor devices using them. The origin of high carrier mobility and the exceptional low leakage current in CAAC-IGZO TFTs, as well as techniques for measuring it, are presented.

The third volume will describe in detail the application of CAAC oxides to display devices – LCD and OLED active matrix circuits, driver circuits and new technologies which apply particularly to flexible displays. Issues of stability and light sensitivity, which are of particular importance in displays, are thoroughly explored and routes to their solution are presented.

In the present volume, the application of CAAC-IGZO to LSI is presented. The book includes a thorough account of the TFT structures exploited and their fabrication, threshold control and switching characteristics, including their extremely low off-state current and

relative immunity to short-channel effects. Then, the application of these components to the most important and relevant electronic subsystems is described: memory, CPUs and FPGAs. The benefits available from CAAC devices in these systems are described – long-term data storage without refresh, higher memory densities and power reduction through adoption of normally-off logic. The design changes which can realise these benefits and the actual performance of circuits are described. In imaging sensors, the low leakage current of CAAC devices allows high-performance global shuttering and on-sensor image processing to be realised, bringing new capabilities to the devices. The volume concludes with an overview of further application fields, including RF tags, X-ray imaging and CODEC systems.

The authors and editors bring to their subject an outstanding breadth of expertise in the research and development of CAAC-IGZO materials, devices and systems, and their account of the subject should provide a definitive source for those seeking to understand and exploit the impact of this developing technology on modern electronics.

Ian Sage
Malvern, UK, 2016

Preface

Entering the 21st century, it seems that the growth of the electronics industry is hitting saturation level, even though it is the largest industry in the world. This is because the amount of energy used by people, which has already become enormous – as reflected in the abrupt climate change in recent years – is going to increase even more with its growth. Especially, the energy consumptions of cloud computing and electronic devices such as smartphones and supercomputers will continue to increase. Therefore, it is not an exaggeration to say that the development of new energy-saving devices has a direct influence on the continued existence of all mankind.

For this reason, we started extensive research on crystalline oxide semiconductors (OS), especially on a *c*-axis-aligned crystalline indium – gallium – zinc oxide (CAAC-IGZO) semiconductor. Due to the economic downturn in the aftermath of the Lehman Brothers' bankruptcy in the autumn of 2008, many companies withdrew from research on this subject, but I never gave up and our research in this area has continued to the present day. One of the most important characteristics of a field-effect transistor (FET) using this wide-gap semiconductor is that the off-state current is on the order of yoctoampère per centimeter (10^{-24}A/cm) (yocto is the smallest SI prefix), which is smaller than that of any other device measured so far. This characteristic effectively reduces the energy consumption, and thus we believe that it coincides with society's need to save energy.

It has been less than 10 years since I started researching and developing oxide semiconductors, but I think that proposing their effectiveness without delay is the first step toward a contribution to humanity. That is why I would like to introduce this book series *Physics and Technology of Crystalline Oxide Semiconductor*, consisting of *Fundamentals*, *Application to LSI*, and *Application to Displays*, even though I know that it cannot be said that every detail is completely covered in the book series.

The book series contains the discovery of CAAC-IGZO by me, Shunpei Yamazaki, one of the editors and authors thereof, as well as the research results on its application obtained at Semiconductor Energy Laboratory Co., Ltd. (SEL), where I serve as president. We have decided to write the experimental facts down in as much detail as possible, and publish models whose principles have not yet been verified. The reason is that I would like to give a couple of hints to readers – graduate students, on-site researchers, and developers – so that they can

conduct further R&D as soon as possible. For these reasons, as well as the limited number of pages, I would like you to accept my deepest apologies for not being able to publish all of the data in these books. Even after the publication of these three books about crystalline oxide semiconductors, I would like to continue making our CAAC-IGZO technology known to the public by conducting further research on it from both engineering and academic points of view.

This book covers a wide range of topics, such as the device physics of FETs using CAAC-IGZO and their applications to LSI.

In the past, Bell Laboratories published a set of books called *The Bell Telephone Laboratories series* about the invention of transistors and research results thereof, which accordingly spread the current concept of transistors throughout the world. We sincerely hope that our books will help to spread the CAAC-IGZO technology just as *The Bell Telephone Laboratories series* helped to popularize the concept of transistors. I think that CAAC-OS, especially CAAC-IGZO, still has many unexplored possibilities and thus more institutions and scientists should research it in cooperation with each other. I am expecting that the CAAC-IGZO which we discovered will flourish in the 21st century by publishing its physical properties and principles, as well as by applying it in the display and LSI fields, especially in energy-saving devices.

So far, we have made some efforts by submitting papers and giving presentations at various conferences about crystalline oxide semiconductors and OS FETs. However, we have never heard of another case where a ceramic was used for an active element on a mass-production basis in Si LSI or displays; thus, many companies (with the exception of Sharp Corporation) will face a lot of difficulties in terms of mass production. Note that a ceramic with an amorphous structure has been proposed before, but it was not put into practical use due to reliability problems. Especially, the great depression following 2008 made many companies quit their R&D of ceramics with an amorphous structure, which was deemed to be fruitless because a FET utilizing amorphous ceramic lacks reliability.

I, Shunpei Yamazaki, observed a TEM image of an IGZO film in front of a TEM screen to find a solution for the reliability issue. At that time, I discovered that a CAAC structure existed in the IGZO film. I thought that the problem of reliability could be solved by using this kind of material, and thus shifted the focus of our R&D to CAAC-IGZO. A FET using this CAAC-IGZO has a high level of reliability, which cannot be said of a FET which uses amorphous IGZO. Thus, a FET with CAAC-IGZO is excellent from a repeatability point of view in that it can be measured and evaluated stably, both on the material and device level. As a result of the stable measurement and evaluation, we discovered that the off-state current is on the order of yoctoamps per centimeter (10^{-24}A/cm), as mentioned above. Additionally, since IGZO has a wide solid-solution phase, we succeeded in fabricating FETs using CAAC-IGZOs having high mobilities of $30 - 70$ cm^2/V-s, thus exceeding 50 cm^2/V-s, by changing the composition ratio and the device structure. A mobility equaling that of an LTPS-FET means that the CAAC-IGZO might be able to not only fight evenly with an LTPS-FET, but also outperform it in the industry. Furthermore, we tried to apply CAAC-IGZO FETs to LSI, something which has never been done before, and discovered that such a FET can operate with a channel length of just $20 - 60$ nm.

Our data has been reviewed by many specialists, but it seems that to help people understand *the true value of the crystalline oxide semiconductor*, there is still a need to further explain the numerous issues concerning fundamental properties, which have not yet been fully understood. Moreover, a lot of people gave us the same advice: to help intellectuals grasp the whole picture

of the technology by publishing a series of at least three books (*Fundamentals*, *Application to LSI*, and *Application to Displays*). Accordingly, I decided to publish them. Note that almost the whole content of these books is based on our experimental data. Hence, please acknowledge SEL and Advanced Film Device Inc. (AFD Inc.), a subsidiary of SEL, as the sources of these books, unless otherwise specified.

During the creation of this book, many people helped and guided us. I would like to express my deepest appreciation especially to Dr. Masahiro Fujita, who has improved the research environment in the field of OS LSI, for being a co-editor of this book, *Application to LSI*, and for training the employees of SEL.

Moreover, during the research and development on which these books are based, as well as during the writing process, many young researchers at SEL also contributed. The names of all the authors involved can be found in the List of Contributors.

We would also like to extend our heartfelt thanks to Dr. Johan Bergquist, Dr. Michio Tajima, Mr. Yukio Maehashi, Mr. Takashi Okuda, and Mr. Jun Koyama for helping us with the writing of this book – by checking for errors and giving us a great deal of advice on how to improve the text.

I was blessed with support and cooperation from many outstanding individuals. I would like to add that I could not have finished these books in such a short period of time without the efforts of Dr. Ian Sage, a Wiley-SID book series editor, who suggested the publication of the books within this time, as well as Ms. Alexandra Jackson and Ms. Nithya Sechin of John Wiley & Sons, Ltd. Last but not least, I would like to express my sincere gratitude to those publishers and authors who allowed us to use their figures as references in these books.

Shunpei Yamazaki
President of Semiconductor Energy Laboratory Co., Ltd.

Acknowledgments

First of all, we would like to thank **Dr. Johan Bergquist**, **Dr. Michio Tajima**, **Mr. Yukio Maehashi**, **Mr. Takashi Okuda**, and **Mr. Jun Koyama**, who encouraged us and gave valuable advice on writing manuscripts.

Furthermore, we would also like to thank many people in a variety of fields for providing data, cooperation in writing manuscripts and English translation, and all other aspects of this book.

Our heartfelt thanks to (in alphabetical order):

Ms. Mayumi Adachi
Ms. Yukari Amano
Mr. Yoshinobu Asami
Mr. Yuji Egi
Mr. Toshiya Endo
Ms. Nana Fujii
Ms. Ai Hattori
Mr. Shinji Hayakawa
Mr. Atsushi Hirose
Mr. Ryota Hodo
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Mr. Masayuki Sakakura
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Mr. Tetsuhiro Tanaka
Ms. Mika Tatsumi
Ms. Yukiko Tojo
Mr. Ryo Tokumaru
Ms. Hitomi Tsurui
Mr. Yuto Yakubo
Mr. Naoto Yamade
Ms. Chiaki Yamura
and many others

Shunpei Yamazaki
Masahiro Fujita

1

Introduction

1.1 Overview of this Book

The three books in this series deal with *c*-axis-aligned crystalline indium–gallium–zinc oxide (CAAC-IGZO), an oxide semiconductor (see Figure 1.1): *Physics and Technology of Crystalline Oxide Semiconductor CAAC-IGZO: Fundamentals* (hereinafter referred to as *Fundamentals*) [1], *Physics and Technology of Crystalline Oxide Semiconductor CAAC-IGZO: Application to LSI* (this book, hereinafter referred to as *Application to LSI*), and *Physics and Technology of Crystalline Oxide Semiconductor CAAC-IGZO: Application to Displays* (hereinafter referred to as *Application to Displays*) [2]. *Fundamentals* describes, for example, the material properties of oxide semiconductors, the formation mechanism and crystal structure analysis of IGZO, the fundamental physical properties of CAAC-IGZO, the electrical characteristics of field-effect transistors (FETs) with CAAC-IGZO active layer (hereinafter referred to as CAAC-IGZO FETs), and comparisons between CAAC-IGZO and silicon (Si) FETs. *Application to Displays* introduces applications of the CAAC-IGZO FET technology to liquid crystal and organic light-emitting diode displays, describing the process flows and characteristics of the FETs, the driver circuits for displays, the technologies for high-definition, low-power, flexible displays, and so on.

This volume, *Application to LSI*, aims to introduce the applications of CAAC-IGZO FET technology to large-scale integration (LSI) and broadly and concisely review the device physics of CAAC-IGZO FETs. On the basis of the distinct material features of these FETs disclosed in *Fundamentals*, such FETs have an attractive application field in LSIs, in addition to the display applications described in *Application to Displays*. Not only focusing on oxide semiconductor material aspects, this book will also describe device design and fabrication using such materials, combination with other technologies, and specific applications (see Figure 1.2).

Physics and Technology of Crystalline Oxide Semiconductor CAAC-IGZO: Application to LSI, First Edition.
Edited by Shunpei Yamazaki and Masahiro Fujita.
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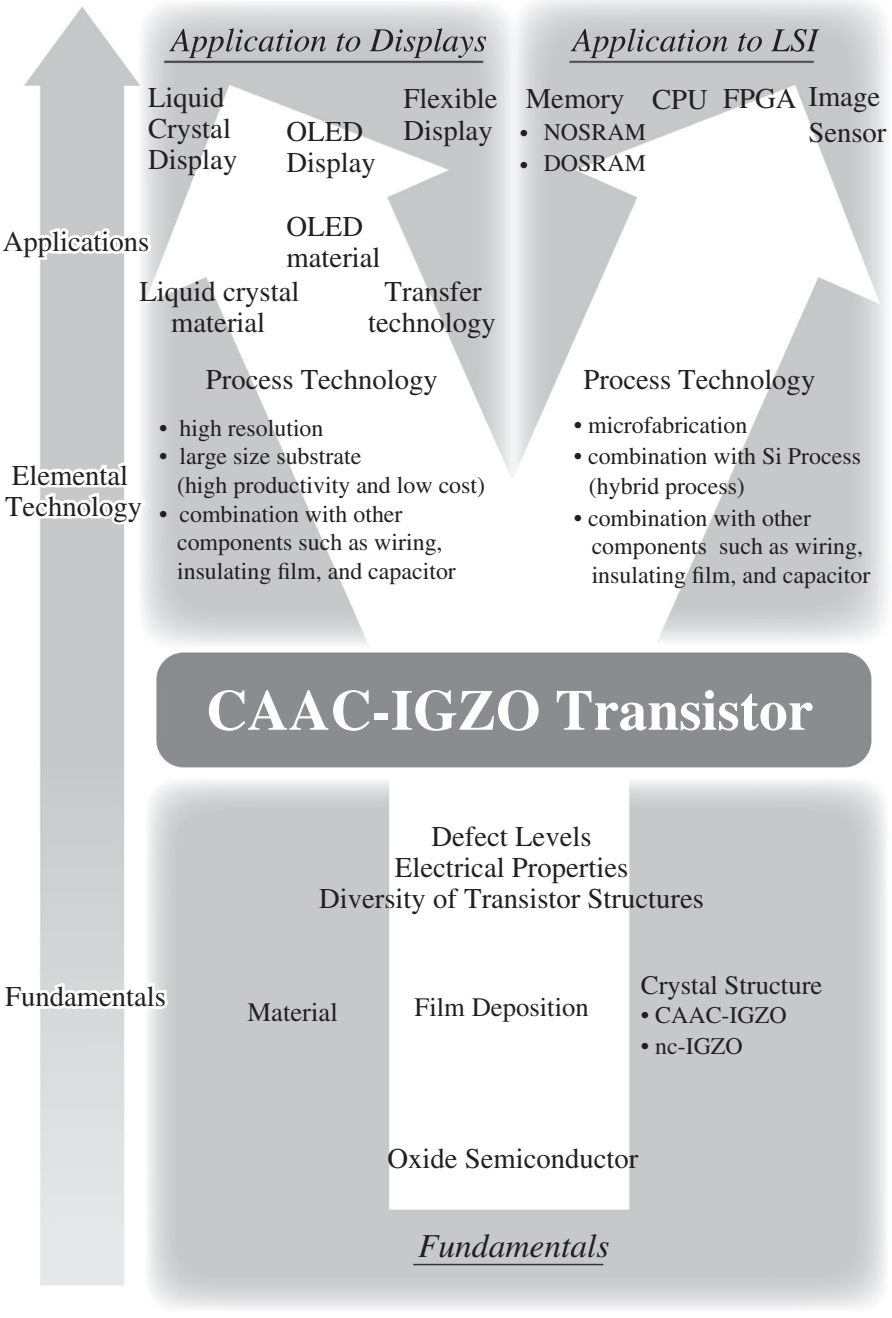


Figure 1.1 Framework and summary of the book series

	Base technology	Problems to be solved	Evaluation
Oxide semiconductor material	Defect control	Increase in purity Impurity control	Structural and elemental analysis Film quality measurement
Oxide semiconductor device	Scale-down technology	Optimization of processes and device structures Consistency with current Si LSI manufacturing	Device physics
Combination with other technologies	Combination with passive elements Hybrid three-dimensional structure of oxide semiconductor and Si elements.	Further reduction in F^2 Development of lower-temperature processes Down-scaling issues	Electrical characteristics
Applications: Internet of Things (IoT), 8K television, mobile devices, etc.		Matching interfaces and performance with other systems	Device size Number of processes Power consumption

Figure 1.2 Scope of this book. The symbol F^2 means the square of the feature size F, used as an index of the memory cell size

Application examples of CAAC-IGZO FET technologies to LSIs are specifically described in the subsequent chapters.

1.2 Background

The integrated circuit (IC) has a huge market [3]. As shown in Figure 1.3, the total market size, including analog, micro, logic, and memory applications, is worth approximately 278 billion US dollars. Here, "micro" applications are microprocessor units (MPUs), microcontroller units (MCUs), and digital signal processors (DSPs); "logic" applications include specified logic and custom logic, such as field-programmable gate arrays (FPGAs) and application-specific integrated circuits (ASICs). CAAC-IGZO FETs address this vast IC market.

1.2.1 Typical Characteristics of CAAC-IGZO FETs

In the LSI field, reduction of power consumption has so far been achieved mainly by scaling down the FETs, employing advanced power management schemes, and more recently, subthreshold driving. Si FETs are currently scaled down to very small technology nodes, for example, gate lengths as small as 14 and 16 nm [4]. Such aggressive downscaling causes

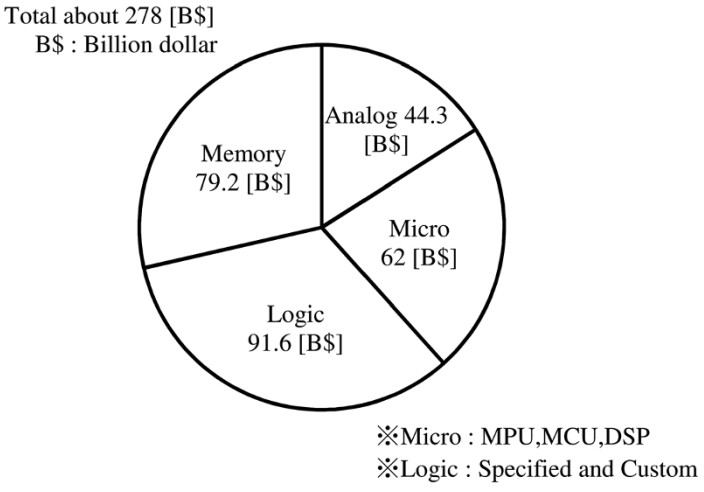


Figure 1.3 Market size of ICs in 2014. *Source*: Adapted from [3]

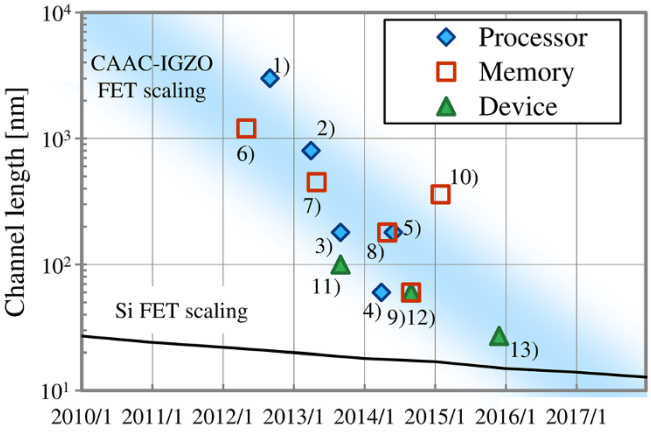
an increase in the FET off-state current (leakage current in the FET in the off state), which poses new obstacles to further reduction of system power [5].

As reported by Kato *et al.* [6], CAAC-IGZO FETs exhibit extremely low off-state current, for example, 1.35×10^{-22} A/μm (135 yA/μm, where y stands for yocto) for a FET with channel length/width of 3/50 μm. In contrast, the off-state current in a single-crystal Si (sc-Si) FET of the same structure and dimensions has an off-state current of 1×10^{-12} A/μm (1 pA/μm), i.e., 10 orders of magnitude larger. When CAAC-IGZO FETs are used in LSI devices, such as dynamic random access memory (DRAM), non-volatile memories, and central processing units (CPUs), their extremely low off-state current will therefore reduce the system power consumption tremendously.

As reported by Matsubayashi *et al*. [7], CAAC-IGZO FETs with a channel node of 20 nm maintain the extremely low off-state current, despite the aggressive downscaling. Figure 1.4 shows the miniaturization progress of CAAC-IGZO and Si FETs during the past four to five years [8]. In the graph, the upper gray band corresponds to the achieved scaling values of CAAC-IGZO FETs, whereas the lower solid line shows the target scaling values of Si FETs disclosed by International Technology Roadmap for Semiconductors [9]. CAAC-IGZO FETs for processors, memories, and devices are denoted by diamond shapes, squares, and triangles, respectively. The number next to each mark corresponds to the conference shown below the graph where the device was disclosed. As shown, the scaling of CAAC-IGZO FETs gradually approaches that of Si FETs in recent years, so if the scaling continues to progress at this speed, it will catch up with that of Si FETs later in 2016 or 2017.

1.2.2 Possible Applications of CAAC-IGZO FETs

CAAC-IGZO FETs can be used in various LSIs (hereinafter called CAAC-IGZO LSIs), for example, in non-volatile memories [10–13], DRAMs [14], normally-off CPUs [15–17], FPGAs [18,19], and image sensors [20,21]. Non-volatile memories and DRAMs employing



Processor:	**Memory:**	**FET:**
1) SSDM 2012	6) IMW 2012	11) SSDM 2013
2) COOL Chips 2013	7) IMW 2013	12) SSDM 2014
3) SSDM 2013	8) IMW 2014	13) IEDM 2015
4) COOL Chips 2014	9) SSDM 2014	
5) VLSI 2014	10) ISSCC 2015	

IEDM : International Electron Devices Meeting
IMW : International Memory Workshop
ISSCC : International Solid-State Circuits Conference
SSDM : International Conference on Solid State Devices and Materials
VLSI : Symposia on VLSI Technology and Circuits

Figure 1.4 Comparison of scaling between CAAC-IGZO FETs and Si FET. *Source*: Adapted from [8].

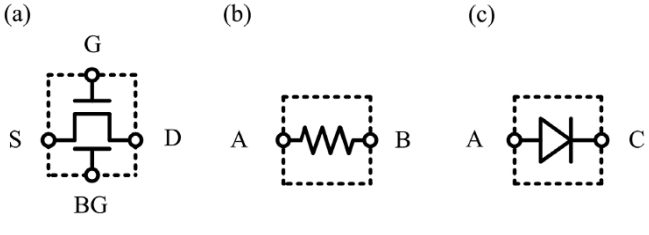


Figure 1.5 (a) CAAC-IGZO FET, an active element with four terminals (source S, drain D, gate G, back gate BG); (b) resistive element, a passive element with two terminals; and (c) diode, a two-terminal passive element with non-linear characteristics

CAAC-IGZO FETs are called non-volatile oxide semiconductor random access memory (NOSRAM) and dynamic oxide semiconductor random access memory (DOSRAM), respectively.

A CAAC-IGZO FET is an active element with four terminals: source, drain, gate, and back gate, as shown in Figure 1.5. New memory technologies that have recently attracted attention

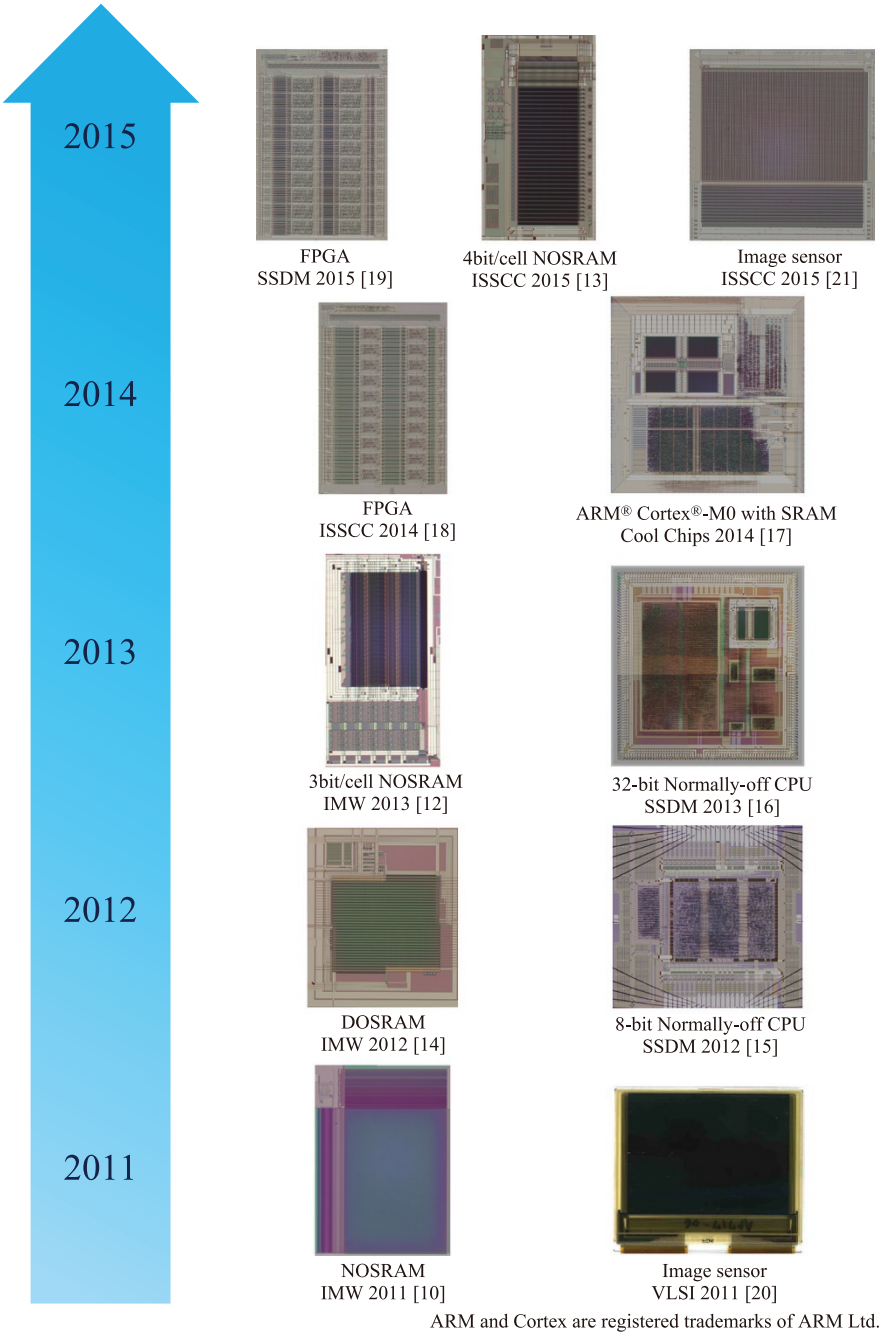


Figure 1.6 Examples of CAAC-IGZO LSIs fabricated between 2011 and 2015

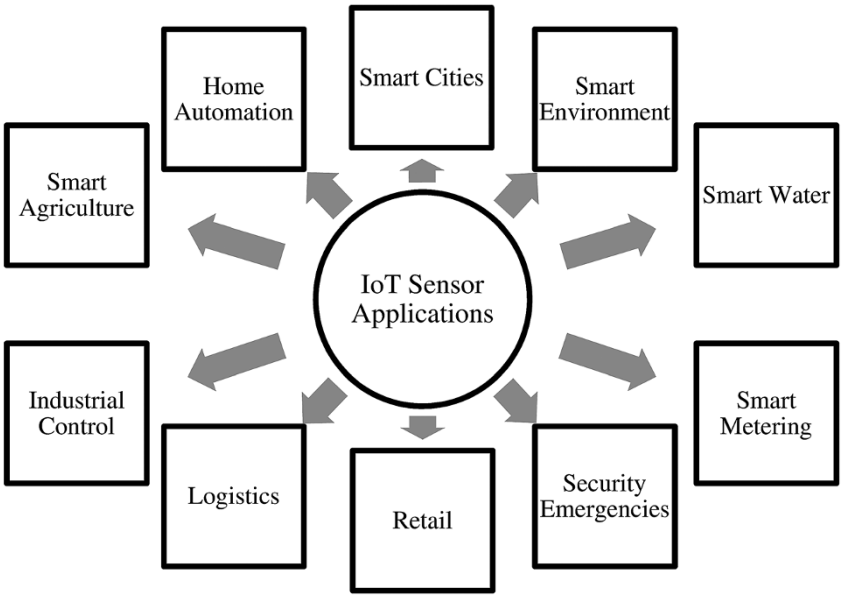


Figure 1.7 Application examples of IoT. *Source*: Adapted from [22,23]

include magnetoresistive random access memory (MRAM), resistive random access memory (ReRAM), phase change random access memory (PCRAM), and ferroelectric random access memory (FeRAM). These are all passive elements with two terminals, whereas CAAC-IGZO FETs with their four terminals may lead to new applications.

Figure 1.6 shows photographs of LSIs with CAAC-IGZO FETs that have been fabricated so far. Below each photograph, the type of LSI and the name of the conference where it was presented are written.

The concept of Internet of Things (IoT) is likely to be realized in the near future. In IoT, LSIs are used in various things to control them and collect and process information through the Internet. LSIs used for IoT should be inexpensive and autonomously powered, i.e., small in size and driven with low power, particularly in the idling state. It is therefore expected that CAAC-IGZO FETs, with their extremely low off-state current, will meet those requirements.

Janusz Bryzek, an advocate of IoT, proposes possible applications of IoT such as logistics, retail, security emergencies, and others (see Figure 1.7) [22,23]. He predicts that a total of one trillion sensors will be used in 2023 (i.e., he forecasts a huge possible market not only for the sensors themselves, but also for the necessary peripheral semiconductor circuits for preprocessing, temporary storage, and wireless transmission).

1.3 Summary of Each Chapter

The device physics, structure, and fabrication process of CAAC-IGZO FETs are briefly explained in Chapter 2, whereas application examples in LSIs and the like are described in and after Chapter 3.

Chapter 2 also includes a review of *Fundamentals*, followed by a description of various CAAC-IGZO FET structures and their basic electrical characteristics, both in general and with emphasis on the low off-state current. CAAC-IGZO FETs are resistant to the downsizing-induced reduction in field-effect mobility or short-channel effect, and unlike sc-Si FETs, the off-state current of CAAC-IGZO FETs does not increase at high temperatures. The possibility of downscaling is illustrated, with results of a CAAC-IGZO FET with channel node of 20 nm [7]. The fabrication process flow of an actual CAAC-IGZO FET with a typical structure is also explained. A hybrid structure that vertically combines Si and CAAC-IGZO FETs is also introduced.

Chapter 3 deals with NOSRAM, where the CAAC-IGZO FET technology is applied to non-volatile memories [10–13]. This non-volatile memory relies on the extremely low off-state current, and can operate at approximately 5 V (i.e., a quarter of the voltage of conventional flash memories). NOSRAM also exhibits an excellent write endurance. While conventional flash memory has a write endurance of approximately 10,000 cycles, NOSRAM endures one trillion writes, achieving a ten-million-fold increase. In addition, the electric potentials can be applied directly to the memory cell during data writing, thus providing accurate control over the accumulated electric charge. Therefore, NOSRAM enables multiple bits in one cell.

Chapter 4 presents DOSRAM in which the CAAC-IGZO FET technology is applied to the DRAM memory cell [14]. Compared with DRAM involving Si, DOSRAM features a long data retention period because the charge stored in the capacitor is hardly lost owing to the extremely low off-state current. Consequently, it requires less frequent refresh operations and therefore consumes less power than its Si FET-based equivalent. For the same reason, electric charges in a capacitor can be stored for a long time even at low capacitance. Accordingly, the capacitance required for data retention may be reduced, which is advantageous in miniaturization.

Chapter 5 describes a normally-off CPU deploying CAAC-IGZO FETs [15–17]. Similar to power gating, the power supply to a circuit stops when unused (the circuit switches to sleep mode) in a normally-off CPU, resulting in low power consumption. When a CPU circuit comprising Si FETs is subject to a power gating operation, there is an overhead in power consumption and performance due to saving and restoring of storage elements in the circuit. Consequently, power gating in short intervals has been problematic because the average CPU power consumption would increase instead. In contrast, a normally-off CPU implemented with CAAC-IGZO FETs reduces the overhead power consumption dramatically by exploiting the extremely low off-state current characteristics of CAAC-IGZO FETs, and shortens the time required for backup and recovery.

Chapter 6 provides an example wherein CAAC-IGZO FETs are applied to FPGAs [18,19]. An FPGA is an LSI that a user can configure after manufacture. In conventional FPGAs, the circuit configuration information is stored in a static random access memory (SRAM) that is used as configuration memory, but SRAM data are generally lost when the power is turned off. Consequently, setting information needs to be stored in the configuration memory every time the power is back on. If a non-volatile memory using a CAAC-IGZO FET replaces this SRAM, setting information is retained even when the power is turned off; thus, the memory does not need restoring in the configuration memory. Moreover, the area and power consumption compared with SRAM may be reduced. Therefore, the incorporation of a CAAC-IGZO FET is expected to produce an FPGA with higher density and lower power consumption. A power gating function can easily be implemented in FPGAs; consequently, turning off unused circuits

may further reduce power consumption. Normally-off operation suitable for fine-grained multi-context structures is also possible by developing the above-mentioned features. Chapter 6 also introduces FPGAs with subthreshold operation, further reducing the power consumption via the lower operating voltage. Finally, the potential development of high-performance computing by combining an FPGA and a CPU, which has recently attracted extensive interest, is discussed.

Chapter 7 presents an example of an image sensor that uses CAAC-IGZO FETs [20,21]. Many of the existing complementary metal–oxide semiconductor (CMOS) image sensors use a rolling shutter mode whereby sensor pixels sequentially capture imaging data row by row. However, this mode exhibits a delay between first and last capturing sensor pixels. Therefore, a fast-moving object yields a distorted image. This delay occurs because captured data get leaked over time and are required to be read out immediately after their capture. When CAAC-IGZO FETs are introduced in an image sensor, the extremely low off-state current of the FETs enables the implementation of a global shutter mode whereby all sensor pixels simultaneously capture data. This off-state current also allows sensor pixels to retain captured data until readout, regardless of any difference in readout timing. Using multiple retention nodes in each sensor pixel allows multiple capture with very short shutter times, an attractive feature in machine vision. Adding an image difference detection function to the sensor pixel gives a motion sensor that performs detection of changes with respect to a reference frame in addition to normal imaging.

Chapter 8 presents other examples of CAAC-IGZO FET applications, demonstrating the versatility of this device. These examples include radio-frequency devices, X-ray detectors, encoder–decoders (CODECs), DC–DC converters (DC denotes direct current), analog programmable devices, and neural networks that may find use in various environments. Further, memory-based computing and an ultra-efficient power gating mechanism are presented.

LSIs with CAAC-IGZO have characteristics of very low off-state current and the associated reduction in system power consumption suggests that CAAC-IGZO LSIs may entirely replace Si LSIs in some applications.

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2

Device Physics of CAAC-IGZO FET

2.1 Introduction

Kimizuka and Mohri [1] first synthesized an indium–gallium–zinc oxide (InGaZn oxide, hereinafter referred to as IGZO) in the 1980s, and revealed its crystal structure. In an IGZO crystal, repeat units, each having an InO_2 layer and a (GaZn)O layer, are periodically stacked to form a layered structure in a phase-equilibrium state (see Figure 2.1) [2]. In 1995, Orita *et al.* [3] examined the conduction characteristics and bandgap of a bulk $InGaZnO_4$ crystal with an ytterbium iron oxide ($YbFe_2O_4$) structure and reported that $InGaZnO_4$ is preferable as a transparent conductive material. Furthermore, Nomura *et al.* [4–6] made a single-crystal IGZO film on an yttria-stabilized zirconia (YSZ) substrate using reactive solid-phase epitaxy with heat treatment at 1400°C; they used the film as an active layer of a field-effect transistor (FET) and reported the FET characteristics. However, a FET with single-crystal IGZO as an active layer has not been put into practical use as of 2016.

Yamazaki *et al.* [7] reported a unique IGZO film with a crystal structure different from that of a single-crystal or polycrystalline IGZO, called a *c*-axis-aligned crystalline IGZO (CAAC-IGZO) film. An $InGaO_3(ZnO)$ crystal in the CAAC-IGZO film has the $YbFe_2O_4$ structure (see *Physics and Technology of Crystalline Oxide Semiconductor CAAC-IGZO: Fundamentals* [8] (hereinafter referred to as *Fundamentals*) for the details). In CAAC-IGZO, the *c*-axes of the crystals are aligned almost perpendicular to the CAAC-IGZO film surface, while the *a*–*b* planes are randomly oriented. In addition, there are no clear grain boundaries between the crystals. Formation of CAAC-IGZO does not require the high temperature of single-crystalline IGZO synthesis (1400°C, see Nomura *et al.* [4]). In addition, instead of epitaxial growth that slowly forms a film, high-speed sputtering can be used for the formation of CAAC-IGZO. A FET having CAAC-IGZO as an active layer (hereinafter referred to as a CAAC-IGZO FET) is characterized by: (1) a low density of defect states due to its crystallinity [9], which offers stable

Physics and Technology of Crystalline Oxide Semiconductor CAAC-IGZO: Application to LSI, First Edition.
Edited by Shunpei Yamazaki and Masahiro Fujita.
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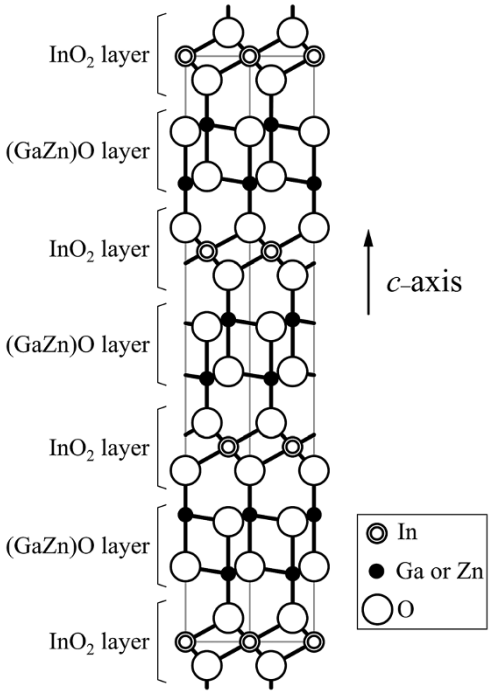

Figure 2.1 Crystal structure of IGZO [$InGaO_3(ZnO)_m$]. InO_2 layers and (GaZn)O layers are periodically stacked to form a layered structure

characteristics; (2) an extremely low off-state current of yoctoamp order (yA/μm, y = 10^{-24}) [10]; and (3) strength against the short-channel effect [11] (here, "off-state current" means the leakage current in the off state). Liquid crystal displays using CAAC-IGZO FETs in the backplanes are already being mass produced [12].

Figure 2.2 shows X-ray diffraction (XRD) spectra of a CAAC-IGZO film. The XRD spectrum in Figure 2.2(a) shows a peak of (009) indicating alignment of the *c*-axes of $InGaO_3(ZnO)$ crystals almost perpendicular to the film surface. In Figure 2.2(b), no diffraction peak is observed in the *a*–*b* plane, suggesting no orientation of the crystal *a*–*b* planes with respect to the film surface (see *Fundamentals* [8] for further details on XRD).

The use of CAAC-IGZO FETs in LSIs proceeds similarly in the display field [13–16]. Miniaturized CAAC-IGZO FETs in an LSI also have the above-mentioned characteristics. The off-state current of a CAAC-IGZO switching FET can be extremely low, which leads to extremely low power consumption by the LSI.

This chapter explains the device physics of a CAAC-IGZO FET. In Section 2.2, its extremely low off-state current will be described. In addition to the basic electrical characteristics, a comparison with a silicon (Si) FET is shown to demonstrate how low the off-state current of the CAAC-IGZO FET is. In fact, it is lower than the detection limit of a normal current-measurement instrument (10^{-13} A), so an original measurement method had to be developed to measure this ultra-low off-state current.

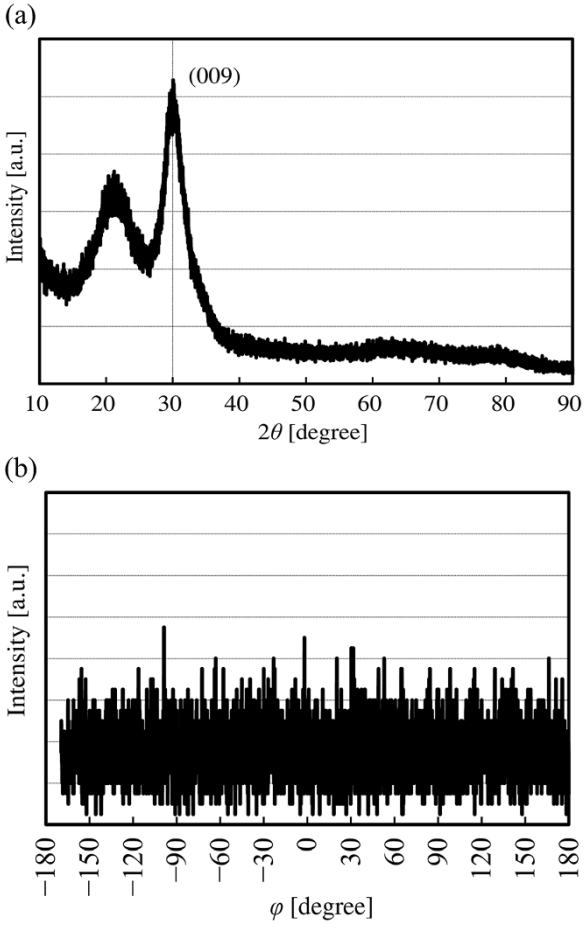

Figure 2.2 XRD spectra of CAAC-IGZO. *Source*: Reprinted from [7], with permission from Wiley

In Section 2.3, a calculation method for estimating off-state currents lower than the detection limit of conventional devices, on the basis of transfer characteristics, is described. This method enables the estimation of I_{cut} (a drain current value I_d at a gate voltage V_g of 0 V) below the detection limit (10^{-13} A). Here, shifting the threshold voltage V_{th} of a CAAC-IGZO FET allows the acquisition of a lower I_{cut} value. The calculation method can be used to find out how much V_{th} should be shifted to obtain a desired I_{cut} value (i.e., the value required for a particular CAAC-IGZO FET application).

In Section 2.4, a technique for controlling the threshold voltage (V_{th}) of a CAAC-IGZO FET is described. The dynamic control of the FET's V_{th} is important not only for a reduction in variation of FET characteristics, but also for use of the extremely low off-state current of the CAAC-IGZO FET in LSI.

Section 2.5 explains the on-state current characteristics of a CAAC-IGZO FET. Although the electron mobility of a CAAC-IGZO FET is much lower than that of a Si FET, the difference in field-effect mobility is reduced for downscaled FETs. While a CAAC-IGZO FET with a

channel length (L) of 1 μm has a field-effect mobility of approximately 10 cm^2/V-s (i.e., 100 times lower than that of a Si FET), miniaturized Si FETs exhibit an increased drift field strength, which accelerates electrons, hence turning them into hot electrons. Hot electrons, in turn, generate phonons, and their drift velocity becomes saturated. That is, the speed of the electrons becomes saturated in a Si FET as the channel gets shorter. In CAAC-IGZO FETs, on the contrary, electrons are not easily accelerated, and do not easily become hot electrons; therefore, a saturation in drift velocity does not occur to the same extent as in a Si FET. As a result, the difference in field-effect mobility versus Si decreases by downscaling. This suggests that CAAC-IGZO FET, if sufficiently small, can replace Si FETs in LSIs.

In Section 2.6, we present a measure to be used against the short-channel effect of a CAAC-IGZO FET. A surrounded-channel (S-ch) structure gives small characteristic degradation. For example, even when a FET has a channel as short as 30 nm and its gate insulator has a thickness as large as 11 nm in equivalent oxide thickness (EOT), characteristic degradation hardly occurs with the S-ch structure.

Section 2.7 introduces a recent scaled-down CAAC-IGZO FET. The CAAC-IGZO FET with a 20-nm node has a cut-off frequency of 34 GHz. In addition, even in the scaled-down FET, the off-state current is extremely low.

The process technology to fabricate LSI devices is introduced in Section 2.8. First, the methods used to fabricate CAAC-IGZO FETs with top-gate top-contact (TGTC) and trench-gate self-aligned (TGSA) structures are explained; then, a hybrid structure in which a CAAC-IGZO FET is placed over a Si FET is described.

2.2 Off-State Current

This section discusses how low the off-state current (leakage current in an off state) of the CAAC-IGZO FET is, compared with that of a conventional Si FET. A CAAC-IGZO FET has an off-state current on the order of yoctoamps (10^{-24} A), below the detection limit of common current measurement (0.1 pA). As possibilities for measuring the off-state current, methods utilizing a FET with increased channel width (W) and the voltage drop of a capacitor are discussed. The reason for the extremely low off-state current of the CAAC-IGZO FET is also discussed theoretically with reference to an energy band diagram.

2.2.1 Off-State Current Comparison between Si and CAAC-IGZO FETs

The off-state currents of Si and CAAC-IGZO FETs are compared with each other (see Figure 2.3). Their drain current–gate voltage (I_d–V_g) characteristics are obtained under −25°C, room temperature (R.T.), and 150°C at a drain voltage V_d of 1 V. As shown in Figure 2.3(a), the off-state current of the Si FET is not lower than the detection limit of 0.1 pA (10^{-13} A), and increases with the measurement temperature. Possible reasons for the off-state current in the Si FET are p–n junction leakage and current generated by interband thermal transition. In contrast, the CAAC-IGZO FET has an off-state current lower than the detection limit regardless of the temperature, as shown in Figure 2.3(b). Because the CAAC-IGZO FET operates in an n-channel accumulation mode, p–n junction leakage does not occur. In addition, CAAC-IGZO has a wide bandgap of approximately 3 eV and few mid-gap levels, so the conduction band carrier generation by interband transitions or excitations from deep levels is also negligible. The detailed mechanisms of the off-state leakage current of CAAC-IGZO FETs

are theoretically discussed in Subsection 2.2.3. Measurement methods developed to detect the yoctoamp-order off-state current of the CAAC-IGZO FET are described in Subsection 2.2.2.

Such an extremely low off-state current, which cannot be obtained in Si FETs, leads to an ultra-low-power device. Various device applications of CAAC-IGZO FET technology have been reported (see Figure 2.4) [18].

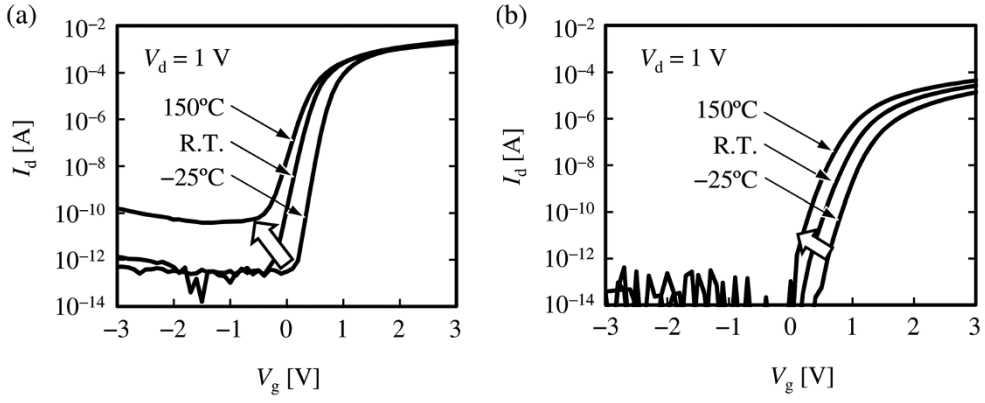

Figure 2.3 Comparison of off-state current between (a) Si FET with $W/L = 0.35\ \mu m/10\ \mu m$ and (b) CAAC-IGZO FET with $W/L = 0.45\ \mu m/10\ \mu m$. *Source*: Adapted from [17]

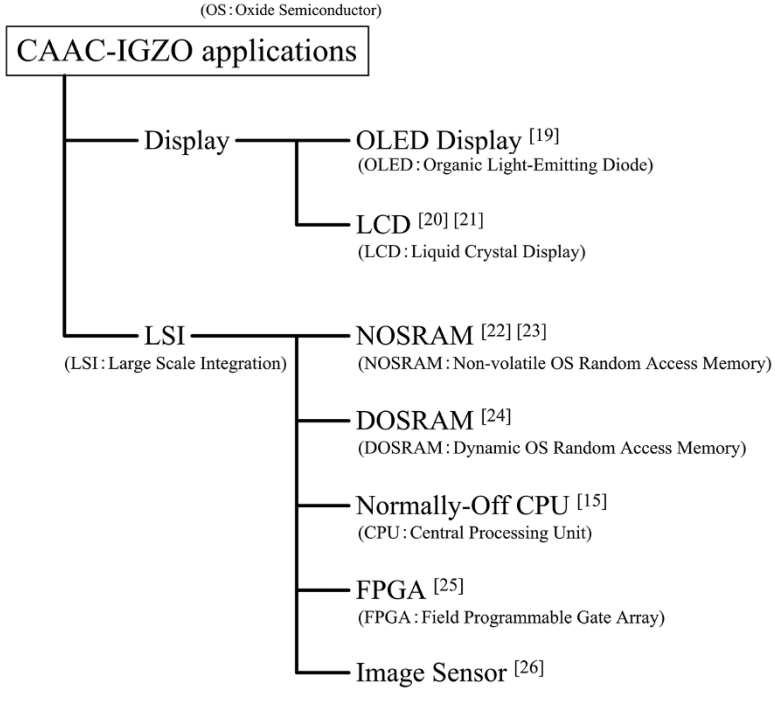

Figure 2.4 Applications of CAAC-IGZO FET technology to various devices. *Source*: Adapted from [18]

2.2.2 *Measurement of Extremely Low Off-State Current*

The extremely low off-state current of the CAAC-IGZO FET is on the order of 10^{-24} A, which is lower than the detection limit (0.1 pA) of common current measurement methods. The off-state current, flowing between a source and a drain when the FET is off, increases in proportion to the channel width. To allow an off-state current measurement, the channel width of the CAAC-IGZO FET is increased to be as wide as 1 m.

Figure 2.5 shows micrographs of a CAAC-IGZO FET with channel length L of 3 μm and channel width W of 1 m [10]. In the left photograph, 20,000 (200 × 100) CAAC-IGZO FETs, each having $W = 50$ μm, are aligned in the 6806 μm × 6878 μm region. The right photograph is an enlarged view of the region enclosed in a square in the left photograph. These CAAC-IGZO FETs are parallel-connected, forming a CAAC-IGZO FET with a total channel width of 1 m.

The cross-sectional structure of one CAAC-IGZO FET is shown in Figure 2.6. This FET has a TGTC structure and employs an overlap structure whereby the gate electrode overlaps with

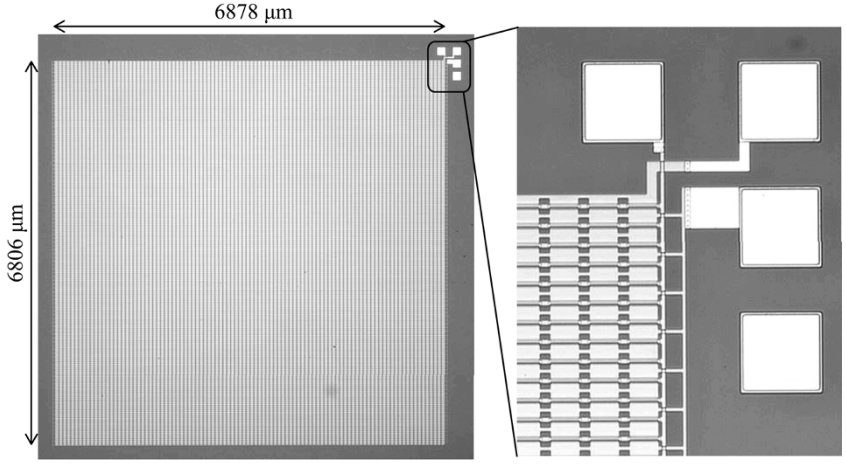

Figure 2.5 Micrographs of the CAAC-IGZO FET with $W = 1$ m. *Source*: Reproduced from [10], with permission of *Japanese Journal of Applied Physics*

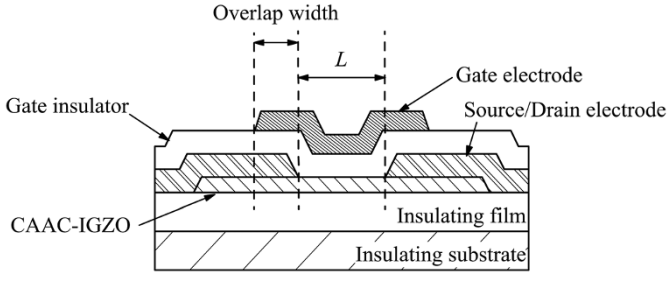

Figure 2.6 Cross-sectional view of the CAAC-IGZO FET

the source and drain electrodes (the overlap width is 2 μm). On a glass substrate, the following films are formed in the order they are listed.

- Base insulating film: 300-nm-thick silicon oxide (amorphous)
- Active layer: 30-nm-thick CAAC-IGZO film
- Source and drain electrodes: 100-nm-thick tungsten
- Gate insulator (sometimes referred to as GI): 100-nm-thick silicon oxide
- Gate electrode: stack of 15-nm-thick tantalum nitride and 135-nm-thick tungsten
- Passivation layer: 300-nm-thick silicon oxide (not shown)

The I_d–V_g characteristics of the CAAC-IGZO FET with $W = 1$ m at $V_d = 3$ V are shown in Figure 2.7. For the measurement, an Agilent 4156C Precision Semiconductor Parameter Analyzer is used. According to Figure 2.7, even though the channel width is as wide as 1 m, the off-state current of the fabricated CAAC-IGZO FET is lower than the detection limit of 0.1 pA.

In order to obtain the off-state current, another method has therefore been developed. To measure the minute current, the small amount of charge moved by the current should be increased to a detectable level. Then, a method of estimating the current by measuring the change in the charge over a long time is developed. Figure 2.8 shows the conceptual diagram of this measurement method. A device under test (here, a CAAC-IGZO FET), which is the element to be measured, is denoted by "DUT." Figure 2.8(a) shows a configuration used to measure the current of the DUT, and Figure 2.8(b) shows the time change of the potential

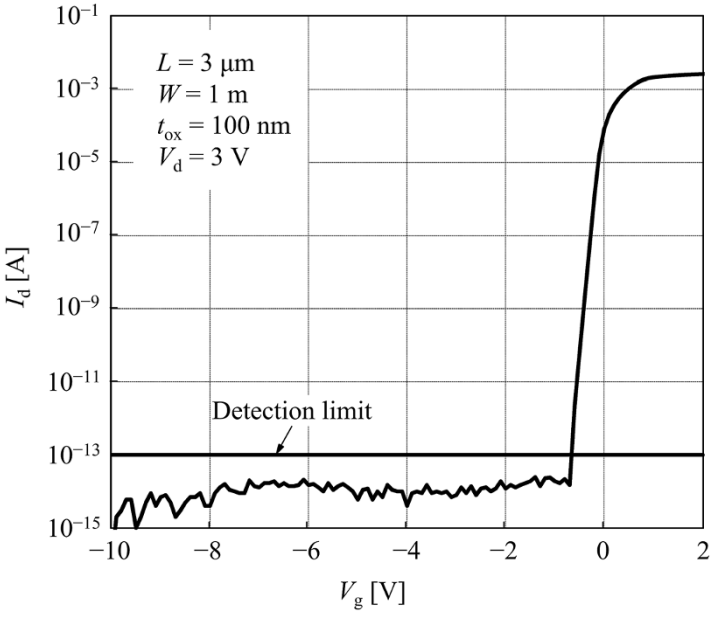

Figure 2.7 I_d–V_g characteristics of the CAAC-IGZO FET with $W = 1$ m. T_{ox} denotes the thickness of the gate insulator. *Source*: Reproduced from [10], with permission of *Japanese Journal of Applied Physics*

V_F of node F connected to the DUT. The leakage current I of the DUT is expressed by the following equation:

$$I = \frac{C_F \Delta V_F}{\Delta t} \tag{2.1}$$

where t and C_F denote the time and capacitance of node F, respectively. The measurement of the time change in potential V_F enables estimation of the off-state current of the DUT.

Equation (2.1) shows the following three important factors for obtaining high measurement accuracy: reduction in C_F, suppression of measurement noise for V_F, and long-term stable measurement. In light of these factors, the circuit configuration, device structure, and measurement environment are constructed.

The constructed circuit configuration comprises the DUT, a reading circuit (source follower), and a programming circuit (see Figure 2.9). In the drawing, G_W and D_W denote the gate and drain electrodes of the programming circuit, respectively; G and S denote the gate and source electrodes of the DUT, respectively; F denotes the floating node; G_R, D_R, and S_R denote the gate, drain, and source electrodes of the reading circuit, respectively; and V_{out} denotes the output potential.

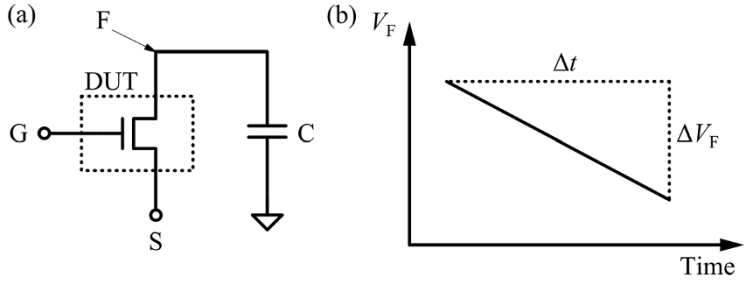

Figure 2.8 Conceptual diagrams of measurement method utilizing voltage drop: (a) circuit diagram; (b) behavior of V_F. *Source*: Adapted from [10]

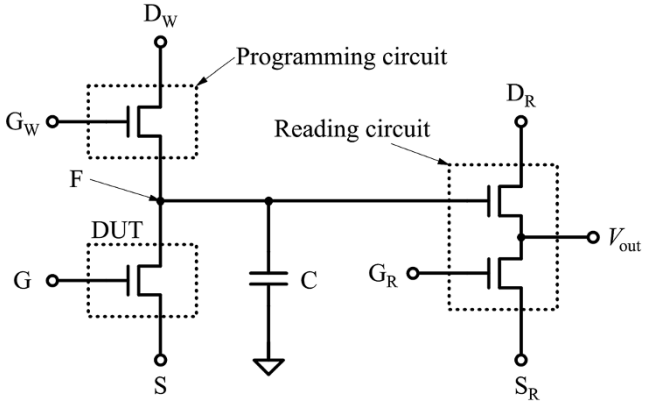

Figure 2.9 Circuit configuration used for measurement. *Source*: Adapted from [10]