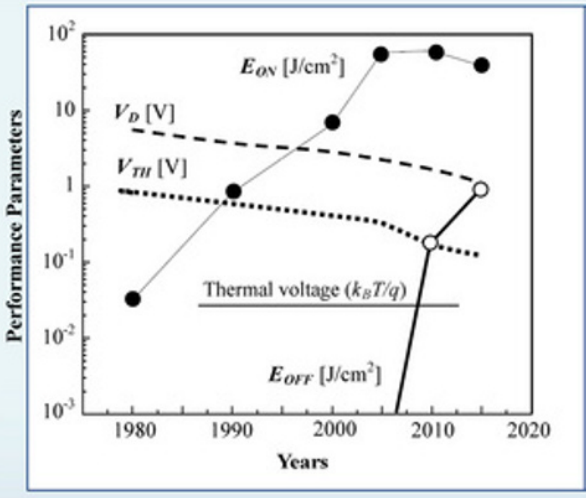
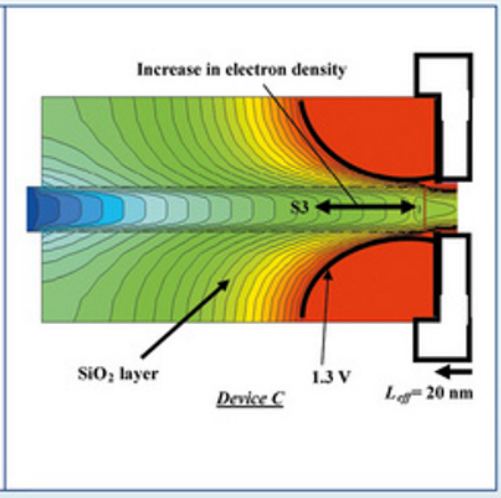
MOS Devices for Low-Voltage and Low-Energy Applications

YASUHISA OMURA | ABHIJIT MALLIK | NAOTO MATSUO





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Preface

The twin goals of low-voltage operation and low power consumption have been pursued for 40 years, since the adoption of the scaling law. In the 1970s, however, the electronics industry did not pay much attention to the scaling law, despite its advantages, because nobody imagined at that time that the industry would grow so rapidly or that the global social infrastructure would be so thoroughly altered by the Internet.

Since the final decade of the twentieth century, the limitations of petroleum-related chemicals and the threat of global warming have compelled industry leaders and scientists to make serious efforts to find solutions. Population pressure is negatively impacting energy resources and global warming, giving the situation particular urgency.

Against this background, many kinds of monitoring technologies using sensors are being developed. However, the power consumption of such products is very high and high-power batteries are needed as a result.

We, the authors, are interested in the development of low-voltage and low-power semiconductor devices to contribute to the energy efficiency of electronic products. In this book we introduce the concept of "low energy" in discussing the above issues. The meaning of "low energy" is described in the following chapters in detail.

We hope that this book will be helpful in developing low-energy device technologies for the electronics industry and the world.

Yasuhisa Omura, Osaka, Japan
Abhijit Mallik, Kolkata, India
Naoto Matsuo, Himeji, Japan

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Part I

INTRODUCTION TO LOW-VOLTAGE AND LOW-ENERGY DEVICES

1

Why Are Low-Voltage and Low-Energy Devices Desired?

The original scaling rule [1] indicated that the dissipation power density (W/cm^2) of an integrated circuit is not changed by scaling [1, 2]. However, this guideline is only really applicable to DRAM devices. In most integrated circuits, the supply voltage is not scaled according to the designer's intent, and devices have faced negative impacts, such as hot-carrier phenomena [3] and negative bias temperature instability (NBTI) phenomena [4], due to high supply voltages [5]. In the twentieth century, central processing unit (CPU) revealed dramatic advances in device performance (high-speed signal processing with increases in data bit length), and the guideline seemed to be ignored (see http://www.depi.itch.edu.mx/apacheco/asm/Intel_cpus.htm, accessed May 18, 2016).

However, in the 1990s, CPU designers noticed the limitations of CPU cooling efficiency, which triggered an urgent and ongoing discussion of low-power device technology. The following possible solutions have been proposed:

- the introduction of a silicon-on-insulator integrated circuit (SOI IC) strategy based on advanced substrate technology [6];
- a multicore strategy [7];
- a low-voltage strategy [8].

These major strategic proposals have led the worldwide electronics industry to the Internet of Things.

Business opportunities based on information technology have increased in the real world without taking account of the issues raised by technologies such as cloud computing [9] and datacenter construction (see http://www.datacenterknowledge.com/,

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accessed May 18, 2016), which have rapidly increased global energy consumption [10]. We must propose viable and innovative ideas on semiconductor device technologies to suppress such global-warming factors.

Information technology has widened perspectives on improving the quality of our future social life. Many companies are creating highly desirable products in the field of sensing technology, such as house monitoring (temperature, humidity, air pollution, fire, human health, security), office monitoring (temperature, humidity, air pollution, fire, security), traffic monitoring (for aspects such as car speed, traffic jams, and accidents), agriculture monitoring (for temperature, humidity, air pollution, rain, wind, lighting, storms), space monitoring (moon, sun, stars, meteorites, and other astronomical phenomena), defense monitoring, and so on. Many of these products use dry batteries or solar power/batteries for 24-hour monitoring. In the case of portable equipment, large batteries are impractical, which has triggered the development of small batteries with high energy density. This is also applicable to cellular phones and smart phones [11].

In battery-powered sensing devices, the battery volume must be small. This may be achieved by lowering the supply voltage, which in turn reduces the battery energy as it is proportional to the square of the voltage. Hence, it is more important to reduce the dissipation energy than the dissipation power for sensing devices. This will be addressed again later. We must, therefore, contribute to the solution of urgent social problems by proposing low-energy devices and integrated circuits.

References

[1] R. H. Dennard, F. H. Gaensslen, H.-N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion implanted MOSFETs with very small physical dimensions," *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 256–268, 1974.

[2] P. K. Chatterjee, W. R. Hunter, T. C. Holloway, and Y. T. Lin, "The impact of scaling laws on the choice of N-channel or P-channel for MOS VLSI," *IEEE Electron Device Lett.*, vol. EDL-1, pp. 220–223, 1980.

[3] T. H. Ning, "Hot-electron emission from silicon into silicon dioxide," *Solid-State Electron.*, vol. 21, pp. 273–282, 1978.

[4] D. K. Schroder and J. A. Babcock, "Negative bias temperature instability: road to cross in deep submicron silicon semiconductor manufacturing," *J. Appl. Phys.*, vol. 94, pp. 1–18, 2003.

[5] B. Kaczer, R. Degraeve, M. Rasras, K. Van de Mieroop, P. J. Roussel, and G. Groeseneken, "Impact of MOSFET gate oxide breakdown on digital circuit operation and reliability," *IEEE Trans. Electron Devices*, vol. 49, pp. 500–506, 2002.

[6] M. Canada, C. Akroul, D. Cawlthron, J. Corr, S. Geissler, R. Houle, P. Kartschoke, D. Kramer, P. McCormick, N. Rohrer, G. Salem, and L. Warriner, "Impact of MOSFET Gate Oxide Breakdown on Digital Circuit Operation and Reliability," IEEE Int. Solid State Circ. Conf. (ISSCC), Dig. Tech. Papers, pp. 430–431, 1999.

[7] T. Chen, R. Raghavan, J. N. Dale, and E. Iwata, "Cell broadband engine architecture and its first implementation – A performance view," *IBM J. Res. Dev.*, vol. 51, pp. 559–570, 2007.

[8] S. Hanson, B. Zhai, K. Bernstein, D. Blaauw, A. Bryant, L. Chang, K. K. Das, W. Haensch, E. J. Nowak, and D. M. Sylvester, "Ultralow-voltage minimum-energy CMOS," *IBM J. Res. Dev.*, vol. 50, pp. 469–490, 2006.

[9] Meil, P., and Grance, T., "The NIST Definition of Cloud Computing," NIST, 2011.

[10] G. Fettweis and E. Zimmermann, "ICT Energy Consumption – Trends and Challenges," The 11th Int. Symp. on Wireless Personal Multimedia Communications (WPMC 2008) (Finland, Sept., 2008), Session WG1: W-GREEN 2008 (I), 2008.

[11] Y. Orikasa, T. Masese, Y. Koyama, T. Mori, M. Hattori, K. Yamamoto, T. Okado, Z.-D. Huang, T. Minato, C. Tassel, J. Kim, Y. Kobayashi, T. Abe, H. Kageyama, and Y. Uchimoto, "High energy density rechargeable magnesium battery using earth-abundant and non-toxic elements," *Sci. Rep.*, vol. 4, Article number: 5622, 2014.

2

History of Low-Voltage and Low-Power Devices

2.1 Scaling Scheme and Low-Voltage Requests

Dennard *et al.* [1] considered the impact of device scaling on device performance. They assumed the device parameters and voltage parameters shown in Table 2.1 when the so-called "constant-field scaling" method was proposed. They assumed the following expression for the metal oxide semiconductor field-effect transistor (MOSFET) drain current:

$$I_D = \left(\frac{W_G}{L_G} \right) C_{ox} \mu_{eff} \left(V_G - V_{TH} - V_D / 2 \right) V_D \tag{2.1}$$

where W_G is the gate width, L_G is the gate length, C_{ox} is the gate capacitance per unit area, μ_{eff} is the carrier mobility, V_G is the gate voltage, V_{TH} is the threshold voltage, and V_D is the drain voltage. Calculation results for the scaling factor (k) are summarized in Table 2.2. They reveal the following features of scaled parameters:

1. The electric field in the device and the averaged carrier velocity are static.
2. Capacitance components, including the depletion layer capacitance, shrink at the rate of $1/k$.
3. The carrier density of the inversion layer in the "ON" state does not change.
4. Drain current (drift current) decreases at the rate of $1/k$.
5. Channel resistance does not change.
6. Switching delay time/device (intrinsic delay time) decreases at the rate of $1/k$.
7. The dissipation power/device decreases at the rate of $1/k^2$.
8. The power-delay product/device shrinks at the rate of $1/k^3$.
9. The dissipation power of devices/unit area does not change.

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Table 2.1 Physical parameters of MOSFET [1].

Parameters	Initial value
t_{ox}	100 nm
N_A	5×10^{15} cm^{-3}
L_G	5 μm
W_G	5 μm
V_D, V_G	20 V

Table 2.2 Constant field scaling and results [1].

Parameters	Scaling factor
Circuit performance	
Device dimension t_{ox}, L_G, W_G	1/k
Doping concentration N_A	k
Voltage V	1/k
Current I	1/k
Capacitance C	1/k
Delay time/circuit VC/I	1/k
Power dissipation/circuit VI	1/k^2
Power density VI/A	1
Interconnection lines	
Line resistance R_L	k
Normalized voltage drop IR_L/V	k
Line response time R_L/C	l
Line current density I/A	k

One important feature that attracted attention in the 1970s was 6. but the concept of "constant-field scaling" was not adopted in industry until after the 1980s [2, 3]. As a result, feature 6. was successful, but features 7.–9. were lost.

From the latter half of the 1990s, the semiconductor industry was able to employ lower supply voltages. The popularity of cellular phones created new demands on the semiconductor industry. As cellular phones must be extremely portable, they need a small battery; this strong demand resulted in low-voltage IC designs. In addition, many battery vendors contributed to battery downsizing and battery energy density enhancement.

Lowering the supply voltage accelerates device scaling. However, the scaling trend ignored the original concept proposed by Dennard *et al.* [1]; the dissipation power of integrated circuits (ICs) per unit area was already much higher than the value estimated by the original scaling concept even though the supply voltage was successfully lowered [4]. The surface temperatures of integrated processor circuits are reaching dangerous values (the intrinsic temperature) [5]. Moreover, we now face the negative influence of several physical device parameters on IC performance because they do not follow any scaling rule. The following are typical of the parameters showing such undesirable behavior:

1. Electric-field induced mobility degradation.
2. Depletion capacitance of poly-Si gate and inversion layer capacitance.

3. Subthreshold swing.
4. Parasitic resistance of devices (gate electrode, source diffusion, drain diffusion, contacts).
5. Leakage current (pn junctions, gate insulator).
6. Threshold voltage.

Issue 1. can basically be overcome using strain technology [6]. Issue 2. can be addressed by using high-κ dielectrics [7], and issue 4. can be improved drastically by the gate-last process [8] and the silicidation process [9]. Issue 6. is aided somewhat by adopting the metal-gate electrode. Issue 5. can be improved by using hetero-junctions and introducing high-κ dielectrics. However, issue 3. remains unresolved because there is no agreement on the design methodology that will allow use of subthreshold operation, or on how to design steep swing devices. Subthreshold logic circuits were proposed to realize the ultimate in low-energy operation [10]. In contrast, steep-swing devices, such as tunnel field-effect transistors (TFETs), were proposed in order to lower the supply voltage and to advance the radio frequency performance of MOSFETs [11]. The TFET device technology is still under investigation, and doesn't yet appear to be a reliable solution for future electronics. It is, however, a leading candidate. This book will discuss the above two concerns; that is, useful applications of subthreshold characteristics and the potential of steep-swing devices.

Before discussing individual solutions, we estimate the power consumption and dissipation energy of conventional complementary metal oxide semiconductor (CMOS) devices. Here we assume the following two equations:

$$\begin{aligned} &\textit{Dissipation power density}\left(\mathrm{W/cm^2}\right) = P_{ON} + P_{OFF} \\ &= r_{ON} f_{clock} \frac{1}{2} C V_D^2 N_{device} + r_{OFF} I_{leak} V_D N_{devices} \end{aligned} \tag{2.2}$$

$$\begin{aligned} &\textit{Dissipation energy density}\left(\mathrm{J/cm^2}\right) = E_{ON} + E_{OFF} \\ &= T_{one-\sec}\left(r_{ON} f_{clock} \frac{1}{2} C V_D{}^2 N_{device} + r_{OFF} I_{leak} V_D N_{devices} \right) \end{aligned} \tag{2.3}$$

where P_{ON} denotes the dissipation power density in the "ON" state, P_{OFF} denotes the dissipation power density in the "OFF" state, N_{device} denotes the number of devices per unit area, r_{ON} denotes the fraction of devices working, r_{OFF} denotes the fraction of devices in standby, f_{clock} denotes the clock frequency, I_{leak} denotes the leakage current of the device, V_D denotes the supply voltage, C denotes the gate capacitance of single CMOS, and $T_{one\text{-}sec}$ denotes the one-second period.

We calculated the dissipation energy of ICs using the equations as shown in Figure 2.1, where we assumed post-1980 device technology. Device parameters assumed in the calculations are summarized in Table 2.3.

Figure 2.1 raises the following key points:

1. E_{OFF} has significantly increased this century;
2. V_{TH} is approaching the thermal voltage;
3. the subthreshold swing should be steep.

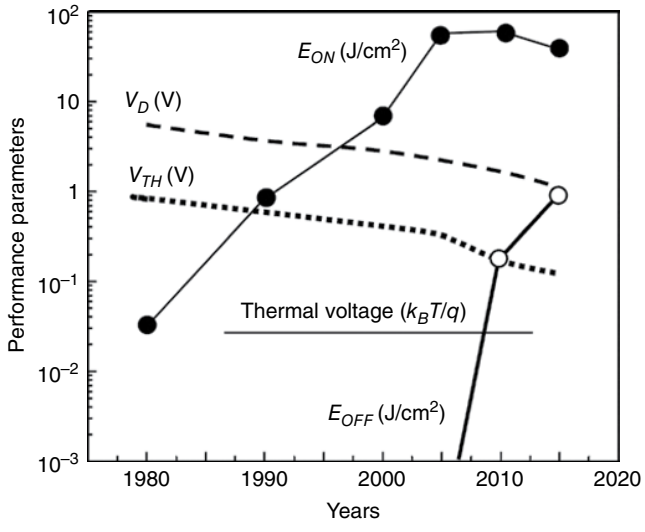

Figure 2.1 Evolution of performance parameters. It is assumed that $r_{ON} = 0.5$, subthreshold swing = 70 mV/dec, and $W_G/L_G = 5$.

Table 2.3 Parameters in simulations.

Years	L_G (nm)	*EOT* (nm)	V_D (V)	V_{TH} (V)	f_{clock} (Hz)	N_{device} (cm^{-2})
1980	2000	50	5.0	1.0	5×10^6	7×10^4
1990	600	20	3.3	0.7	1×10^8	1×10^6
2000	200	8.0	2.5	0.5	1×10^9	5×10^6
2005	55	2.2	2.0	0.4	3×10^9	8×10^7
2010	30	1.4	1.5	0.2	3×10^9	3×10^8
2015	24	1.1	1.0	0.15	3×10^9	5×10^8

EOT: equivalent oxide thickness.

The calculation results suggest that we must continuously lower the supply voltage, but also that we will reach its floor (the thermal voltage, ~26 mV at 300 K) [12].

2.2 Silicon-on-Insulator Devices and Real History

In the 1980s, silicon-on-insulator (SOI) substrate technology emerged and was commercialized. Before the 1980s, silicon-on-sapphire (SOS) substrate technology was the major material for SOI device applications [13]. The SOI substrate was studied in order to develop high-speed switching devices because the silicon-on-sapphire metal oxide semiconductor field-effect transistor (SOS MOSFET) had a much smaller parasitic capacitance beneath the source and drain diffusions than the bulk MOSFET. However, the SOS material had some serious issues, such as the autodoping of Al from the sapphire substrate and high-density defects near the Si/sapphire interface. The Si-based SOI substrate technology basically replaced the SOS substrate technology because the latter's shortcomings could not be ignored by 1990.

Before the 1990s, the electronics industry focused on the signal processing speed of ICs. After the 1990s, however, the industry had to pay attention to IC dissipation power because energy concerns were becoming more pronounced. Accordingly, leading scientists and engineers studied the low-power performance of SOI ICs with low-power dissipation closely [14], and many companies began studies to develop high-performance ICs [15]. Many scientists and engineers, however, remained skeptical about whether sub-100 nm gate silicon-on-insulator complementary metal oxide semiconductor (SOI CMOS) technology was actually suitable for creating the ICs needed in the twenty-first century because no aggressive technical vision had been published. Such negative perceptions were familiar in the electronics industry because nobody predicted the dramatic expansion of worldwide use of mobile phones and tablet PCs. Before specific ICs for mobile phones were developed, the power supply voltage was still high (~3 V). The voltage level was too high to yield a 100 nm gate SOI CMOS with fully depleted mode operation; the parasitic bipolar phenomenon induces the single-transistor latch [16], and many engineers were very skeptical as to the reality of scaled fully depleted silicon-on-insulator metal oxide semiconductor field-effect transistors (SOI MOSFETs). Fortunately, in the latter half of the 1990s, many businessmen began to use cellular phones and notebook PCs, forcing the electronics industry to overcome the historical barrier of power-supply voltage. This breakthrough gave the fully depleted SOI devices a good business opportunity with the result that they are used in many commercial electronics products.

Dr. K. Izumi and his group developed the ITOX-SIMOX (Internal Thermal OXidation-Separation by IMplanted OXygen) substrate [17], which can be applicable to scaled CMOS devices, and one of the editors (Omura) and his colleagues in NTT Laboratories demonstrated the potential of the 100 nm gate SOI CMOS IC with fully depleted components [18]. With the development of the oxygen ion-implanter, commercially viable SIMOX substrates became possible [19], SIMOX substrates were used to fabricate SOI devices and circuits in the laboratories of many companies. After the 1980s, other SOI substrate fabrication technologies, such as ELTRAN® and UNIBOND®, were also proposed [20–23], and have now entered commercialization. In the twenty-first century, companies that could catch this technology trend are doing well, while those that could not faltered.

Let us consider how we can use the low-power performance of SOI MOSFETs. Intrinsic switching delay time (τ) and dissipation power (P_{ON}) of SOI MOSFET are given by

$$Switching\ delay\ time\left(\tau / Tr\right) = \left(L_G W_G C_{ox} + L_G W_G C_{S,D}\right)\frac{V_D}{I_D} + C_P \frac{V_D}{I_D} \tag{2.4}$$

$$Dissipation\ power\left(P_{ON} / Tr\right) = V_D I_D \tag{2.5}$$

where C_{ox} denotes the gate capacitance per unit area, $C_{S,D}$ denotes the source and drain capacitance per unit area, and C_P denotes the parasitic capacitance except $C_{S,D}$. Energy dissipated by a single switching event (τP_{ON}) can be estimated as

$$Power \cdot Delay\ product\left(P_{ON} \cdot \tau / Tr\right) = \left\{\left(L_G W_G C_{ox} + L_G W_G C_{S,D}\right) + C_P\right\} V_D^2. \tag{2.6}$$

Estimated dissipation power of IC (P_{ON}) is given by using the clock frequency (f_{clock}):

$$P_{ON} = N_{device} f_{clock} \left\{\left(L_G W_G C_{ox} + L_G W_G C_{S,D}\right) + C_P\right\} V_D^2 \tag{2.7}$$

We must also take account of the standby power of the IC (P_{OFF}), given by

$$P_{OFF} = N_{device} I_{leak} V_D \tag{2.8}$$

As a result, the overall dissipation power (P_{total}) of the LSI is given by

$$\begin{aligned} P_{total} &= P_{ON} + P_{OFF} \\ &= N_{device} f_{clock} \left\{ \left(L_G W_G C_{ox} + L_G W_G C_{S,D} \right) + C_P \right\} V_D^2 + N_{devices} I_{leak} V_D \end{aligned} \tag{2.9}$$

In the above expressions, the terms that are significantly different from the estimated values of the bulk MOSFET are those that include $C_{S,D}$ and C_p. In SOI CMOS devices, we can predict a reduction in I_{leak} due to a reduction in effective junction area, suppression of I_{leak} increases based on better subthreshold swing values, and C_p reductions due to shrinkage of device isolation area, resulting in the suppression of increases in P_{total}. However, as the IC designer is always seeking to enhance signal-processing performance, P_{ON} will increase due to the increase in the value of $N_{device} f_{clock}$. When the IC designer lowers the MOSFET threshold voltage to raise the switching speed, I_{leak} inevitably increases.

Recent P_{OFF} values are comparable to P_{ON} due to I_{leak}. IC designers are suffering from this conundrum. Therefore, one of the primary concerns of this book is how to suppress P_{OFF} as well as whether we can find applications that do not need high-speed performance.

In Part II, we review the fundamentals of conventional MOSFETs, SOI MOSFETs, and TFETs. This part will help readers to follow easily the discussions in the other parts. In Part III, we discuss how we can use the low-energy performance of bulk MOSFETs and how we can apply such devices to low-energy circuits. In Part IV, we review the low-energy performance potential of fully depleted SOI MOSFETs and introduce examples. In Part V, we address the low-energy performance potential of cross-current tetrode (XCT) SOI MOSFETs, which were proposed to realize extremely low energy circuits. In Part VI, the low-energy potential of quantum-effect devices, proposed by taking account of geometrical aspects, is considered. In Part VII, we discuss comprehensively how we can suppress the energy dissipation by using TFETs, one of the more recent quantum-effect devices. In Part VIII, finally, we briefly compare the performance of various devices and review considerations described in Part III to Part VII. We also address the latest low-energy devices, circuit applications, and future perspectives.

References

[1] R. H. Dennard, F. H. Gaensslen, H.-N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion implanted MOSFETs with very small physical dimensions," *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 256–268, 1974.

[2] P. K. Chatterjee, W. R. Hunter, T. C. Holloway, and Y. T. Lin, "The impact of scaling laws on the choice of N-channel or P-channel for MOS VLSI," *IEEE Electron Device Lett.*, vol. EDL-1, pp. 220–223, 1980.

[3] T. H. Ning, "Hot-electron emission from silicon into silicon dioxide," *Solid-State Electron.*, vol. 21, pp. 273–282, 1978.

[4] C. Fiegna, H. Iwai, T. Kimura, S. Nakamura, E. Sangiorgi, and B. Riccò, "Monte Carlo Analysis of Hot Carrier Effects in Ultra Small Geometry MOSFETs," Int. Workshop on VLSI Process and Device Modeling: VPAD (Nara, 1993), pp. 102–103, 1993.

[5] S. M. Sze and K. K. Ng, "Physics of Semiconductor Devices," 3rd ed. (John Wiley & Sons, Inc., 2007), p. 20 and p. 26.

[6] Z. Y. Cheng, M. T. Currie, C. W. Leitz, G. Taraschi, E. A. Fitzgerald, J. L. Hoyt, and D. A. Antoniadis, "Electron mobility enhancement in strained-Si n-MOSFETs fabricated on SiGe-on-insulator (SGOI) substrates," *IEEE Electron Device Lett.*, vol. 22, pp. 321–323, 2001.

[7] V. Misra, G. Lucovsky, and G. Parsons, "Issues in high-κ gate stack interfaces," *MRS Bull.*, vol. 27, pp. 212–216, 2001.

[8] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. McIntyre, P. Moon, J. Neirynck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, and K. Zawadzki, "A 45 nm Logic Technology with High-κ+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193 nm Dry Patterning, and 100% Pb-free Packaging," IEEE IEDM Tech. Dig. (Washington DC, 2007), pp. 247–250, 2007.

[9] J. Kedzierski, P. Xuan, E. H. Andersonf, J. Bokor, T.-J. King, and C. Hu, "Complementary Silicide Source/Drain Thin-Body MOSFETs for the 20 nm Gate Length Regime," Tech. Dig. IEEE IEDM (San Francisco, 2000) pp. 57–60, 2000.

[10] S. A. Vitale, P. W. Wyatt, N. Checka, J. Kedzierski, and C. L. Keast, "FESOI process technology for sub-threshold-operation ultralow-power electronics," *Proc. IEEE*, vol. 98, pp. 333–342, 2010.

[11] K. K. Bhuwalka, J. Schulze, and I. Eisele, "Performance enhancement of vertical tunnel field-effect transistor with SiGe in the layer," *Jpn. J. Appl. Phys.*, vol. 43, no. 7A, pp. 4073–4078, 2004.

[12] R. Landauer, "Irreversibility and heat generation in the computing process," *IBM J. Res. Dev.*, vol. 5, pp. 183–191, 1961.

[13] J.-P. Colinge, "Silicon-on-Insulator Technology: Materials to VLSI," 3rd ed. (Kluwer Academic Publishers, 2004), pp. 12–13.

[14] M Itoh, Y. Kawai, S. Ito, K. Yokomizo, Y. Katakura, Y. Fukuda, F. Ichikawa, "Fully Depleted SIMOX SOI Process Technology for Low-Power Digital and RF Device," Proc. 10th Int. Symp. Silicon on Insulator Technology and Devices (The Electrochem. Soc.) (Washington DC, 2001) Vol. 2001-3, pp. 331–336, 2001.

[15] J.-P. Colinge, "Silicon-on-Insulator Technology: Materials to VLSI," 3rd ed. (Kluwer Academic Publishers, 2004), Chapter 8.

[16] C.-E. D. Chen, M. Matloubian, R. Sundaresan, B. Mao, C. C. Wei, and G. P. Pollack, "Single-transistor Latch in SOI MOSFETs," *IEEE Electron Device Lett.*, vol. 9, pp. 636–638, 1988.

[17] S. Nakashima, Y. Omura, and K. Izumi, "A High-Quality SIMOX Wafer and Its Application to Ultrathin-Film MOSFETs," Proc. 5th Int. Symp. on SOI Technol. Dev. (The Electrochem. Soc., 1992) Vol. 92–13, pp. 358–367, 1992.

[18] Y. Omura, S. Nakashima, K. Izumi, and T. Ishii, "0.1-μm-Gate, Ultrathin-Film CMOS Devices Using SIMOX Substrate with 80-nm-Thick Buried Oxide Layer," 1991 IEEE Int. Electron Devices Meeting, Tech. Dig., pp. 675–678, 1991.

[19] K. Izumi, Y. Omura, and S. Nakashima, "Promotion of practical SIMOX technology by the development of a 100 mA-class high-current oxygen implanter," *Electron. Lett*, vol. 22, no. 15, pp. 775–777, 1986.

[20] T. Yonehara, K. Sakaguchi, and N. Sato, "Epitaxial layer transfer by bond and etch back of porous Si," *Appl. Phys. Lett.*, vol. 64, pp. 2108–2110, 1994.

[21] T. Yonehara and K. Sakaguchi, "ELTRAN®; novel SOI wafer technology," *Jpn. Soc. Appl. Phys. Int.*, no. 4, pp. 10–16, 2001.

[22] M. Bruel, "Application of hydrogen ion beams to silicon on insulator. Material technology," *Nucl. Instrum. Methods Phys. Res., Sect. B*, vol. 108, pp. 313–319, 1996.

[23] G., Celler "Smart Cut®, A guide to the technology, the process, the products," SOITEC, Press Release, July 1, 2003.

3

Performance Prospects of Subthreshold Logic Circuits

3.1 Introduction

The possibility of lowering the dissipation energy is addressed for the following conventional device technologies:

- multithreshold circuits [1];
- power management [2];
- subthreshold logic [3].

In a multithreshold circuit, designers can assume that different circuit blocks can have different threshold voltages. They can set low threshold voltages for high-speed circuit blocks and high threshold voltages for low-power circuit blocks. This technique is widely applied to commercial integrated circuits (ICs). In the case of power management, the power supply is switched in individual circuit blocks; this is a more recent technique, used most often in mobile electronics. In some cases the signal-processing speed might be degraded. In the case of subthreshold logic, conventional device technology is assumed but the supply voltage is lowered to the threshold voltage or much less. The logic circuit works in the subthreshold current range. In the last century this design approach was applied to control circuits in wrist watches [4].

3.2 Subthreshold Logic and its Issues

As described in the previous section, circuit designers initially used multithreshold devices and power management to reduce the dissipation power of ICs. These ideas are not innovative, as they are mere extensions of conventional techniques. Reducing dissipation power by lowering

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the supply voltage is also a conventional design guideline, where metal oxide semiconductor field-effect transistors (MOSFETs) are used in the conventional manner in the circuit.

On the other hand, the subthreshold logic and near-subthreshold logic approaches are quite different from the design idea of focusing on "ON" state performance. Circuit designers are now paying close attention to the quasi-"OFF" state. Rather than using the high impedance of the device, they target extremely low currents for logic circuits.

When we apply the subthreshold current of the MOSFET to low-power circuits, we must be careful of the noise issue, the variability of characteristics, and nonlinearity of *I-V* characteristics. Verma *et al.* recently addressed these points in detail [5].

3.3 Is Subthreshold Logic the Best Solution?

Low-power logic circuits, like the subthreshold logic circuits described in the previous section, are now commercialized as ICs for wrist watches [6]; such circuits were the concern of a small group of engineers and the design methodology was not familiar to most engineers. There was skepticism regarding whether a design technique based on subthreshold logic circuits would be utilized frequently.

In order to change these negative impressions, one of the editors (Omura) proposed the cross-current tetrode-silicon-on-insulator metal oxide semiconductor field-effect transistor (XCT-SOI MOSFET) [7, 8]. One of its advantages is the fact that we can basically design the required circuits by applying conventional design methodology in terms of supply voltage and device layout patterns. We can reduce the dissipation power by two orders when the "source potential floating effect" is significant. The most important point in the device design is that we can simply assume the stable saturation region of the drain current despite a very low drain current comparable to the subthreshold level. Details of device characteristics and aspects are described in Part V. We therefore still have many choices for reducing dissipation energy in various circuit applications.

References

[1] T. Douseki, J. Yamada, and H. Kyuragi, "Ultra Low-Power CMOS/SOI LSI Design for Future Mobile Systems," Dig. of Technical Papers, Int. Symp. on VLSI Circuits, June 2002, pp. 6–9, 2002.

[2] S. Mutoh, T. Douseki, Y. Matsuya, T. Aoki, S. Shigematsu, and J. Yamada, "1-V power supply high-speed digital circuit technology with multithreshold-voltage CMOS," *IEEE J. Solid-State Circuits*, vol. 30, pp. 847–854, 1995.

[3] S. A. Vitale, P. W. Wyatt, N. Checka, J. Kedzierski, and C. L. Keast, "FESOI process technology for subthreshold-operation ultralow-power electronics," *Proc. IEEE*, vol. 98, pp. 333–342, 2010.

[4] E. Vittoz, B. Gerber, and F. Leuenberger, "Silicon-gate CMOS frequency divider for the electronic wrist watch," *IEEE J. Solid-State Circuits*, vol. 7, pp. 100–104, 1972.

[5] N. Verma, J. Kwong, and A. P. Chandrakasan, "Nanometer MOSFET variation in minimum energy subthreshold circuits," *IEEE Trans. Electron Devices*, vol. 55, pp. 163–174, 2008.

[6] C. Piguet, "Low-Power CMOS Circuits –Technology, Logic Design and CAD Tools," (CRC Press, 2006), Chapter 1.

[7] Y. Omura, Y. Azuma, Y. Yoshioka, K. Fukuchi, and D. Ino, "Proposal of preliminary device model and scaling scheme of cross-current tetrode silicon-on-insulator metal-oxide-semiconductor field-effect transistor aiming at low-energy circuit applications," *Solid-State Electron.*, vol. 64, pp. 18–27, 2011.

[8] Y. Omura and D. Sato, "Mechanisms of low-energy operation of XCT-SOI CMOS devices – Prospect of sub-20-nm regime," *J. Low Power Electron. Appl.*, vol. 4, pp. 14–25, 2014.

Part II

SUMMARY OF PHYSICS OF MODERN SEMICONDUCTOR DEVICES

4

Overview

This part describes the fundamentals of metal oxide semiconductor (MOS) device physics. First, we describe the physics of bulk metal oxide semiconductor field-effect transistors (MOSFETs). Then, some important physics related to silicon-on-insulator metal oxide semiconductor field-effect transistors (SOI MOSFETs) (partially depleted SOI MOSFET, fully depleted SOI MOSFET, FinFET, Triple-gate FET, gate-all-around MOSFET) are introduced, followed by the theoretical basis of tunnel field-effect transistors (TFETs).

The accumulation condition, the depletion condition, and the inversion condition in bulk MOSFET are explained. Threshold voltage and subthreshold swing are also explained as important parameters of MOSFET [1, 2]. In SOI MOSFETs, aspects of partially depleted (PD) SOI MOSFETs and fully depleted (FD) SOI MOSFETs are outlined [3, 4]. The reasons why FinFET, Triple-gate FET, and Gate-All-Around (GAA) MOSFET are superior to the PD and FD SOI MOSFETs are discussed [5, 6], and their details are described in the following parts. Finally, we discuss the physics of TFETs [7].

It is obvious that we must minimize the subthreshold swing (SS) value of the MOS device in designing device parameters for low-power applications. However, there is still some controversy regarding the issue of whether the subthreshold issue is the substantial problem in overcoming the stand-by power issue. In many MOS devices we can face a simultaneous increase in the band-to-band tunneling (BTBT) current around the source and drain junctions because there must be shallow junctions in bulk devices or an extremely thin semiconductor layer in silicon-on-insulator (SOI) devices in order to suppress short-channel effects. Readers will find that MOS devices with steep swing values and low BTBT current values often suffer from the low drivability. We must therefore take account of such tradeoff issues in optimizing the device's performance even when we discuss the low-standby energy concept and device applications. The following chapters review theoretical models of various MOSFETs.

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References

[1] S. M. Sze and K. K. Ng, "Physics of Semiconductor Devices," 3rd ed. (John Wiley & Sons, Inc., 2007), Chapter 6.
[2] Y. Tsividis, "Operation and Modeling of the MOS Transistor," 2nd ed. (Oxford University Press, 1999).
[3] J.-P. Colinge, "Silicon-on-Insulator Technology: Materials to VLSI," 3rd ed. (Kluwer Academic Pubishers, 2004).
[4] T. Sakurai, A. Matsuzawa, T. Douseki (eds.) "Fully-Depleted SOI CMOS Circuits and Technology for Ultralow-Power Applications," (Springer, 2006), pp. 23–58.
[5] J.-P. Colinge (ed.) "FinFETs and Other Multi-Gate Transistors" (Springer, 2008), Chapters 1 and 2.
[6] S. Deleonibus (ed.) "Electronic Device Architectures for Nano-CMOS Era –from Ultimate CMOS Scaling to beyond CMOS Devices" (Pan Stanford Publishing, 2009).
[7] A. C. Seabaugh, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. IEEE*, vol. 98, pp. 2095–2110, 2010.

5

Bulk MOSFET

5.1 Theoretical Basis of Bulk MOSFET Operation

Figure 5.1 shows a schematic cross section of a bulk n-channel metal oxide semiconductor field-effect transistor (MOSFET). In the following, we assume an n-channel MOSFET. As there is a single channel inside the body, there are three current flows at the onset of inversion: the front-channel current, the band-to-band tunneling (BTBT) currents at the front interface of the drain junction, and double injection currents at the source junction. In the subthreshold region, the subthreshold current is at the front interface. This chapter focuses on the DC characteristics of bulk MOSFET, and presents a theoretical analysis of the subthreshold and post-threshold current characteristics as an aid to low-energy device design.

5.2 Subthreshold Characteristics: "OFF State"

5.2.1 Fundamental Theory

Many papers have described the basic features of the subthreshold characteristics of bulk MOSFETs [1, 2]. The input capacitance consists of four components in series: (i) the capacitance of the gate insulator; (ii) the capacitance of the channel depletion layer; (iii) the capacitance of the depletion layer of the source junction (this is available when there exists potential difference between the source terminal and the substrate), and (iv) the capacitance of the depletion layer of the drain junction [2].

In the subthreshold regime, the drain current (Figure 5.2) is given by

$$I_{D(sub)} = I_{D(sub),front} + I_{D(sub),other} \tag{5.1}$$

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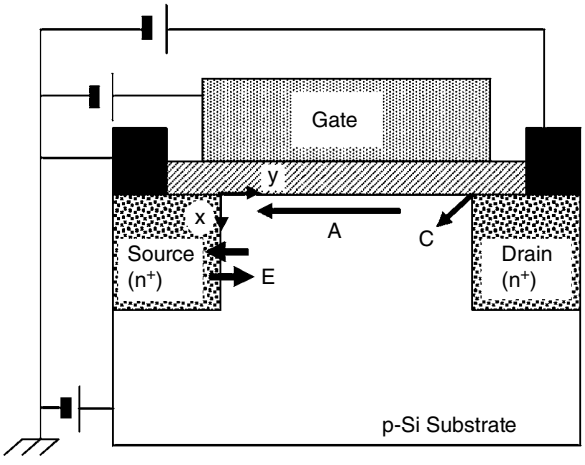

Figure 5.1 Bulk MOSFET – cross-section and operation. A: normal front channel, C: avalanche and band-to-band tunnel current (front side), and E: double injection on parasitic bipolar action.

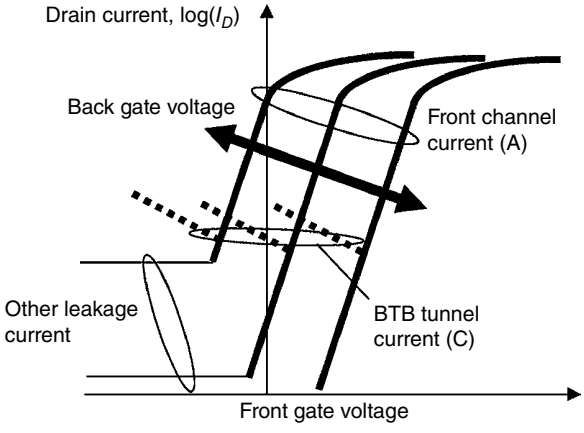

Figure 5.2 Subthreshold and off-state current characteristics of bulk MOSFET. (With kind permission from Springer Science + Business Media: Fully-Depleted SOI CMOS Circuits and Technology for Ultralow-Power Applications, 2006, pp. 48–58, Yasuhisa Omura (edited by T. Sakurai, A. Matsuzawa, and T. Douseki),© 2006 Springer.)

where $I_{D(sub),front}$ is the subthreshold current near the front interface and $I_{D(sub),other}$ is the combined current attributable to parasitic phenomena, such as a simple avalanche at the drain junction [3, 4], BTBT at the drain junction [5, 6] and the generation-recombination (GR) process [7]. For simplicity, this discussion will focus on $I_{D(sub),front}$. For an n-channel MOSFET, it is

$$I_{D(sub),front} = -qAD_n \frac{dn}{dy} = qAD_n \frac{n(0) - n(L_{eff})}{L_{eff}} \tag{5.2}$$

where A is the cross-sectional area of the channel, q is the elementary charge, D_n is the diffusion constant of electrons, L_{eff} is the effective channel length, and $n(0)$ and $n(L_{eff})$ are the electron concentrations at the edges of the source and drain, respectively. They are given by

$$n(0) = n_i \exp\left[\frac{\left(E_F - E_i + q\varphi_{s,front}\left(x=0, y=0\right)\right)}{k_B T}\right] \tag{5.3}$$

and

$$n\left(L_{eff}\right) = n_i \exp\left[\frac{\left(E_F - E_i + q\varphi_{s,front}\left(x=0, y=0\right) - qV_D\right)}{k_B T}\right] \tag{5.4}$$

where $\varphi_{s,front}$ is the surface potential at the top surface, n_i is the intrinsic carrier density, E_F is the Fermi level, E_i is the intrinsic Fermi level, k_B is the Boltzmann's constant, and T is the temperature in K. If we assume the effective channel depth to be $k_B T/qE_s$ [8], where E_s is the surface electric field [9], the subthreshold current can be written as

$$I_{D(sub),front} = \mu_n\left(\frac{W_{eff}}{L_{eff}}\right)q\left(\frac{k_B T}{q}\right)^2\left(\frac{n_i^2}{N_A}\right)\left\{1-\exp\left[\frac{-qV_D}{k_B T}\right]\right\}\frac{\exp\left[\frac{q\varphi_{s,front}}{k_B T}\right]}{E_S} \tag{5.5}$$

where μ_n is the electron mobility calculated from the Einstein relation $D_n = \mu_n k_B T/q$, N_A is the doping concentration of substrate, W_{eff} is the channel width, and V_D is the drain voltage. We can derive the following basic expression for the subthreshold swing (SS) from Eq. (5.5) if we neglect the influence of interface states for simplicity.

$$SS = \left(\frac{kT}{q}\right)\ln(10)\left\{1+\frac{C_s}{C_{ox}}\right\} \tag{5.6}$$

where

$$C_s = \frac{\varepsilon_s}{W_D} \tag{5.7}$$

C_{ox} $(=\varepsilon_{ox}/t_{ox})$ is the capacitance of the gate oxide layer, C_s is the depletion capacitance of the substrate, t_{ox} is the thickness of the gate oxide layer, ε_s is the permittivity of semiconductor, and W_D is the depletion layer width. As seen in Eq. (5.6), the basic expression for SS depends on doping concentration of the substrate, gate oxide layer thickness, permittivity of the gate oxide layer, and permittivity of the substrate.

The main conclusions that can be drawn from Eq. (5.6) are:

- Influence of gate oxide thickness (t_{ox}) on SS. One of the most common ways to suppress short-channel effects is to reduce t_{ox}, which makes C_s/C_{ox} small, as shown by Eq. (5.6). This means that the t_{ox} leads to the straightforward reduction of SS.

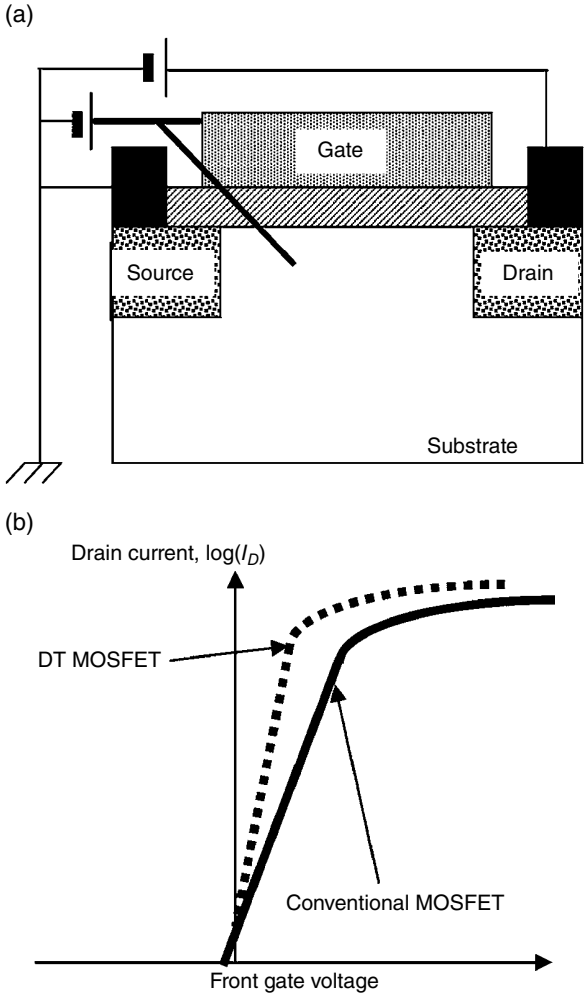

Figure 5.3 Dynamic-threshold MOSFET. (a) Cross section and (b) characteristics.

- Influence of doping concentration (N_A) on *SS*. Another common way to suppress short-channel effects is to increase N_A. This often causes *SS* to increase. To prevent that, t_{ox} should also be reduced when N_A is increased.
- Influence of substrate potential on *SS:* dynamic-threshold (DT) MOSFET operation (Figure 5.3). The substrate potential is often set to a certain value. In that case, *SS* is almost independent of the front gate voltage, but depends on the device parameters. In a dynamic-threshold MOSFET [10], the substrate terminal is connected to the front gate electrode; so, the substrate potential increases with the front gate voltage. This increase reduces the built-in potential of the source junction, thereby increasing the channel current. So, a simplified expression for the subthreshold current of a dynamic threshold MOSFET is

$$I_{D(sub),DT} = I'_{D(sub),front} C_0 \exp\left[\frac{qV_{FG}}{mk_BT}\right] \tag{5.8}$$

where

$$I'_{D(sub),front} = \mu_n \left(\frac{W_{eff}}{L_{eff}} \right) q \left(\frac{k_B T}{q} \right)^2 \left(\frac{n_i^2}{N_A} \right) \left\{ 1 - \exp\left[\frac{-qV_D}{k_B T} \right] \right\} \frac{\exp\left[\frac{q\varphi_{s,front}\left(x=0, y=0, V_{FG}\right)}{k_B T} \right]}{E_S} \tag{5.9}$$

C_0 is a constant, m is the ideality factor ($m > 1$), and $\varphi_s(x = 0, y = 0, V_{FG})$ is the surface potential modified by V_{FG}. It should be noted that the subthreshold channel region depends on the initial surface condition of the device because the front gate voltage does not change the band structure near the top surface drastically. This is an important aspect of the dynamic threshold MOSFET. An approximate expression for the *SS* of a dynamic threshold MOSFET is

$$SS = \eta \left(\frac{k_B T}{q} \right) \ln(10) \left[1 + \frac{C_s}{C_{ox}} \right] \tag{5.10}$$

where $\eta < 1$ and C_s is given by Eq. (5.7).

- Drain-induced barrier lowering (DIBL) (front interface) (Figure 5.4). In a short-channel bulk MOSFET, DIBL [11] near the source junction at the front interface significantly degrades the SS. The reason for this is that the drain-induced lateral electric field extends quite far into the channel region. There are two ways to suppress the DIBL: one is to make N_A higher, and the other is to replace the gate oxide with a high-κ material. However, the former degrades the SS because C_s increases in Eq. (5.6). Therefore, the pocket ion-implantation technique [12] is frequently introduced in order to suppress the extension of the drain-induced lateral electric field.

5.2.2 *Influence of BTBT Current*

Band-to-band tunneling often occurs in the gate-drain overlap region [13]. It is sometimes called the gate-induced drain leakage (GIDL) current. For MOSFETs with a thin gate oxide, it has a significant influence on DC and AC operation [14]. An empirical expression for this current is [15]

$$I_{D(sub),others} = A_0 E_{SS} \exp\left[\frac{-B_0}{E_{SS}} \right] \tag{5.11}$$

where A_0 and B_0 are constants that depend on the device parameters and E_{SS} is the surface electric field of the gate overlap region. As the gate oxide of recent MOSFETs tends to be very thin, the electric fields of the gate-drain and drain-source overlap regions are higher than those of past devices. As a result, the contribution of the BTBT current to the subthreshold characteristics is apt to be significant [16].

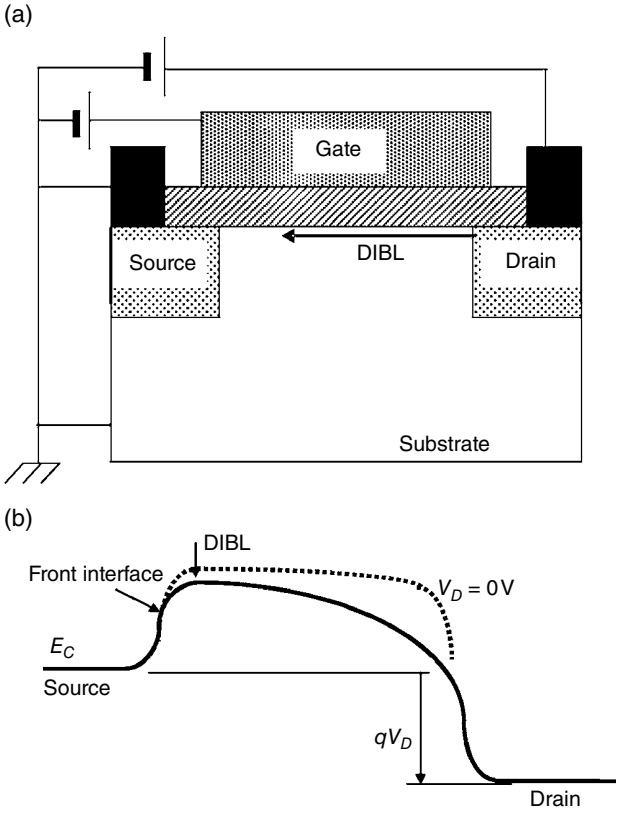

Figure 5.4 Drain-induced barrier lowering phenomenon in the bulk MOSFET. (a) Schematic view of DIBL and (b) impact of DIBL on the surface potential profile.

5.2.3 Points to Be Remarked

The "OFF state" current in the subthreshold region limits the standby power of the MOSFET even when the threshold voltage is sufficiently high. In the case of the bulk MOSFET, the reverse-biased leakage current generated at a large metallurgical junction area, the weak avalanche-based current, and the BTBT current around the gate-overlapped region of the drain diffusion region shares a large part of the total leakage current. These are apt to increase when the short-channel effects are suppressed because the suppression of the short-channel effects raises the local electric field around the drain diffusion. Therefore the lowering of the drain voltage is requested for the purpose of the suppression of those leakage current components. These points will be discussed again later.

5.3 Post-Threshold Characteristics: "ON State"

5.3.1 Fundamental Theory

In the post-threshold regime, the drain current is given by

$$I_{D(post)} = I_{D(post),front} + I_{D(post),other} \tag{5.12}$$

where $I_{D(post),front}$ is the inversion channel current along the front interface and $I_{D(post),other}$ is the parasitic current, which consists of the leakage current of the reverse-biased drain junction [17], a parasitic bipolar current [18], and an avalanche current [19]. The discussion below focuses on $I_{D(post),front}$.

In practice, the post-threshold channel current consists mainly of the drift current, where carriers are accelerated by the drain-to-source electric field. It is analyzed in the conventional gradual channel approximation. The expression for the drain current of the bulk MOSFET is derived below.

We start from the Ohmic relation

$$I_{D(post),front} = -W_{eff}\mu_n Q_n(V)\frac{dV(y)}{dy} \tag{5.13}$$

where $V(y)$ is the local channel potential and $Q_n(V)$ is the local electronic charge density. This is the expression for the local current inside the device, if we neglect the diffusion and other currents like the generation-recombination current.

We obtain the following relation for $Q_n(V)$ from Poisson's equation for the channel region [20]:

$$\begin{aligned} Q_n &= \text{total induced charge density of semiconductor} - \text{depletion charge density of substrate,} \\ &= -C_{ox}\left(V_{FG} - V_{FB,front} - \varphi(0) - V\right) + qN_A W_D\left(\varphi(0) + V\right) \end{aligned} \tag{5.14}$$

Integrating it from source to drain based on the current continuity, we obtain the following expression for $I_{D(post),front}$:

$$I_{D(post),front} = \left(\frac{W_{eff}}{L_{eff}}\right)\mu_n C_{ox}\left[V_{FG} - V_{TH}^{*} - \frac{V_D}{2}\right]V_D + (optional - term) \tag{5.15}$$

where

$$V_{TH}^{*} = V_{FB,front} + \varphi_{s,front}(x=0, y=0) + \frac{\sqrt{2q\varepsilon_S N_A \varphi_{s,front}(x=0, y=0)}}{C_{ox}} + (optional - term) \tag{5.16}$$

When the doping level near the surface is not so high, substituting the new expression for $Q_n(V)$ into the Ohmic relation (5.13), and assuming current continuity, yield the following expression for $I_{D(post)}$, front:

$$I_{D(post),front} = \left(\frac{W_{eff}}{L_{eff}}\right)\mu_n C_{ox}\left[V_{FG} - V_{TH,front} - \frac{V_D}{2}\right]V_D \tag{5.17}$$

where the threshold voltage of a MOSFET ($V_{TH,front}$) is

$$V_{TH,front} = V_{FB,front} + \varphi_{s,front}(x=0, y=0) + \frac{qN_A W_D\left[\varphi_{s,front}(x=0, y=0)\right]}{C_{ox}} \tag{5.18}$$

The saturated drain current ($I_{D(post)sat}$) is given by:

$$I_{D(post)sat} = \left(\frac{W_{eff}}{2(1+\alpha)L_{eff}} \right) \mu_n C_{ox} \left[V_{FG} - V_{TH,front} \right]^2 \tag{5.19}$$

where α is the factor depending on the substrate doping concentration profile. When the substrate has a uniform doping profile and its doping concentration is not so high, $\alpha \to 0$. The drain current of the bulk MOSFET on the saturation condition is basically independent of the drain voltage (V_D) as far as short-channel effects are not seen. Other important factors are discussed below.

5.3.2 Self-Heating Effects

Powered devices suffer from self-heating effects as shown in Figure 5.5. In the bulk MOSFET, the thermal conductivity of the substrate is not so high [21]. According to simulations [22], the temperature near the drain junction quickly rises to 100 °C. Since self-heating effects degrade the surface mobility of carriers, they must be taken into account. In electrostatic-discharge (ESD) protection circuits, self-heating effects reduce the temperature margin for the second breakdown. So, adequate thermal paths must be added during metallization.

If we need to take into account the influence of self-heating effects on drain current, we have to use the following expression for the mobility [23]:

$$\mu_{n(self-heating)} = C_1 \left[T_0 + \theta I_{D(post),front} V_D \right]^{-\delta} \tag{5.20}$$

where C_1 is a constant, T_0 is room temperature, and θ and δ are fitting parameters.

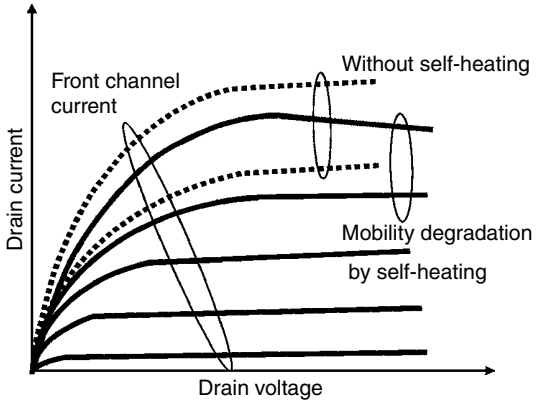

Figure 5.5 I_D-V_D characteristics of bulk MOSFET.

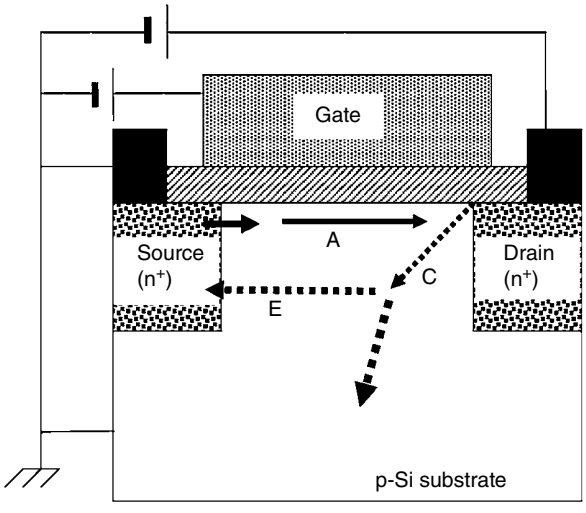

Figure 5.6 Parasitic bipolar action in the n-channel bulk MOSFET. Avalanche-induced holes (C) are injected into the source (E), and electrons are injected into the body (A). This positive feedback loop turns on parasitic bipolar action.

5.3.3 Parasitic Bipolar Effects

When the drain-to-source voltage is high, the electric field around the drain pn junction takes a high value. In the depletion region around the drain pn junction, a weak avalanche multiplication of carriers takes place. In that case, as shown in Figure 5.6, most holes generated near the drain are absorbed to the bulk substrate ("C" in Figure 5.6) and they are collected at the substrate terminal; this is the so-called "substrate current." However, some holes flow into the source junction ("E" in Figure 5.6). When the substrate resistivity is high, the body potential automatically rises by the substrate current. When the "forward-biased" current is made at the source junction, it works as the "base current" of the "NPN" parasitic bipolar transistor. This frequently results in a fatal "burnout" phenomenon.

5.4 Comprehensive Summary of Short-Channel Effects

Considering a simple phenomenalistic model of short-channel effects, we obtain

$$V_{TH} = V_{FB,front} + f_{DIBL}\varphi_{s,front}\left(x=0,y=0\right) + f_{CS}\frac{qN_A W_D\left[\varphi_{s,front}\left(x=0,y=0\right)\right]}{C_{ox}} - \eta V_{BG}^{'} \tag{5.21}$$

where f_{DIBL} is the DIBL factor, f_{CS} is the charge-sharing factor, and η is the factor expressing the impact of the substrate bias effect.

References

[1] S. M. Sze and K. K. Ng, "*Physics of Semiconductor Devices*," 3rd ed. (John Wiley & Son, Inc., 2007), Chapter 6.

[2] Y. Tsividis, "*Operation and Modeling of the MOS Transistor*," 2nd ed. (Oxford University Press, 1999).

[3] S. M. Sze and G. Gibbons, "Avalanche breakdown voltages of abrupt and linearly graded p-n junctions in Ge, Si, GaAs, and GaP," *Appl. Phys. Lett.*, vol. 8, pp. 111–113, 1966.

[4] G. Merckel, F. Van de Wiele, W. Engl, and P. Jespers, "*NATO Course on Process and Device Modeling for Integrated Circuit Design*," (Noordhoff, 1975), p. 725.

[5] L. Esaki, "New phenomenon in narrow germanium p-n junctions," *Phys. Rev.*, vol. 109, p. 603, 1958.

[6] E. O. Kane, "Theory of tunneling," *J. Appl. Phys.*, vol. 32, pp. 83–91, 1961.

[7] W. Shockley and W. T. Read, Jr., "Statistics of the recombination of holes and electrons," *Phys. Rev.*, vol. 87, pp. 835–842, 1952.

[8] S. M. Sze and K. K. Ng, "*Physics of Semiconductor Devices*," 3rd ed. (John Wiley & Sons, Inc., 2007), p. 314.

[9] S. M. Sze and K. K. Ng, "*Physics of Semiconductor Devices*," 3rd ed. (John Wiley & Sons, Inc., 2007), p. 301.

[10] F Assaderaghi, D. Sinitsky, S. A. Parke, J. Boker, P. K. Ko, and C. Hu, "A Dynamic Threshold Voltage MOSFET (DTMOS) for Ultra-Low Voltage Operation," Tech. Dig. Int. Electron Devices Meeting (San Francisco, Dec., 1994) pp. 809–812, 1994.

[11] G. W. Taylor, "Subthreshold conduction in MOSFET's," *IEEE Trans. Electron Devices*, vol. 25, pp. 337–350, 1978.

[12] T. Hori, "A 0.1 μm CMOS Technology with Tilt-Implanted Punchthrough Stopper (TIPS)," Tech. Dig., IEEE IEDM (San Francisco, 1994) pp. 75–78, 1994.

[13] E. Takeda, H. Matsuoka, and S. Asai, "A Band to Band Tunneling MOS Device (B^2T-MOSFET)–A Kind of 'Si quantum Device'," Tech. Dig., IEEE IEDM (San Francisco, 1988) pp. 402–405, 1988.

[14] M. Chan, J. Lin, S. N. Shih, T.-C. Wu, B. Huang, J. Yang, and P.-I. Lee, "Impact of gate-induced drain leakage on retention time distribution of 256 Mbit DRAM with negative wordline bias," *IEEE Trans. Electron Devices*, vol. 50, pp. 1036–1041, 2003.

[15] H.-J. Wann, P.-K. Ko, and C. Hu, "Gate-Induced Band-to-Band Tunneling Leakage Current in LDD MOSFETs," Tech. Dig. IEEE IEDM (San Francisco, 1992) pp. 147–150, 1992.

[16] J. Chen, F. Assaderaghi, P.-K. Ko, and C. Hu, "The enhancement of Gate-Induced-Drain-Leakage (GIDL) current in short-channel MOSFET and its application in measuring lateral bipolar current gain," *IEEE Electron Device Lett.*, vol. 11, pp. 572–574, 1992.

[17] S. M. Sze and K. K. Ng, "*Physics of Semiconductor Devices*," 3rd ed. (John Wiley & Sons, Inc., 2007), pp. 90–114.

[18] L. Wakeman, "Silicon-gate CMOS chips gain immunity to SCR latchup," *Electronics*, vol. 56, pp. 136–140, 1983.

[19] S. M. Sze and K. K. Ng, "*Physics of Semiconductor Devices*," 3rd ed. (John Wiley & Sons, Inc., 2007), pp. 104–106.

[20] S. M. Sze and K. K. Ng, "*Physics of Semiconductor Devices*," 3rd ed. (John Wiley & Sons, Inc., 2007), pp. 298–303.

[21] D. Sharma, J. Gautier, and C. Merckel, "Negative resistance in MOS devices," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 378–380, 1978.

[22] D. Sharma and K. Ramanathan, "Modeling thermal effects on MOS I-V characteristics," *IEEE Electron Device Lett.*, vol. EDL-4, p. 362, 1983.

[23] R. van Langevelde and F. M. Klaassen, "Accurate Drain Conductance Modeling for Distortion Analysis in MOSFETs," Tech. Dig. IEEE IEDM (Washington, D. C., 1997) pp. 313–316, 1997.

6

SOI MOSFET

6.1 Partially Depleted Silicon-on-Insulator Metal Oxide Semiconductor Field-Effect Transistors

The partially depleted (PD) n-channel silicon-on-insulator metal oxide semiconductor field-effect transistor (SOI MOSFET) has a quasineutral region in the silicon-on-insulator (SOI) layer as shown in Figure 6.1. This configuration is very similar to that of the bulk metal oxide semiconductor field-effect transistor (MOSFET) except for the buried oxide layer beneath the device region. Therefore, most operation characteristics are similar to those of the bulk MOSFET. However, the device has a few different characteristics from the bulk MOSFET, such as the kink in I_D versus V_D characteristics [1–4] and the body-floating characteristics [1–4]; that is, the potential of the quasineutral region is not fixed to a specific potential. When the potential of the quasineutral region floats, the potential of the quasineutral region of the SOI MOSFET cannot respond quickly to changes in the gate electrode and the drain electrode, which slows the operation of the partially depleted SOI MOSFET [5].

When a positive bias is applied to the substrate, the depletion layer expands from the bottom surface of the silicon layer, which yields an optional leakage current path on the bottom surface of the silicon layer. We have to increase the body doping concentration near the bottom surface of the silicon layer in order to suppress this optional leakage current [6]. When a high positive bias is applied to the substrate, the silicon body can be fully depleted [6]. When the full depletion of the silicon body is held, the SOI MOSFET exhibits the specific characteristics described in the following section.

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