## ---MOS DEVICES FOR LOW-VOLTAGE AND LOW-ENERGY APPLICATIONS

YASUHISA OMURA | ABHIJIT MALLIK | NAOTO MATSUO







## MOS DEVICES FOR LOW-VOLTAGE AND LOW-ENERGY APPLICATIONS

## MOS DEVICES FOR LOW-VOLTAGE AND LOW-ENERGY APPLICATIONS

Yasuhisa Omura Kansai University, Japan

**Abhijit Mallik** University of Calcutta, India

Naoto Matsuo Hyogo Pref. University, Japan





This edition first published 2017 © 2017 John Wiley & Sons Singapore Pte. Ltd.

#### Registered Office

John Wiley & Sons Singapore Pte. Ltd., 1 Fusionopolis Walk, #07-01 Solaris South Tower, Singapore 138628

For details of our global editorial offices, for customer services and for information about how to apply for permission to reuse the copyright material in this book please see our website at www.wiley.com.

All Rights Reserved. No part of this publication may be reproduced, stored in a retrieval system or transmitted, in any form or by any means, electronic, mechanical, photocopying, recording, scanning, or otherwise, except as expressly permitted by law, without either the prior written permission of the Publisher, or authorization through payment of the appropriate photocopy fee to the Copyright Clearance Center. Requests for permission should be addressed to the Publisher, John Wiley & Sons Singapore Pte. Ltd., 1 Fusionopolis Walk, #07-01 Solaris South Tower, Singapore 138628, tel: 65-66438000, fax: 65-66438008, email: enquiry@wiley.com.

Wiley also publishes its books in a variety of electronic formats. Some content that appears in print may not be available in electronic books.

Designations used by companies to distinguish their products are often claimed as trademarks. All brand names and product names used in this book are trade names, service marks, trademarks or registered trademarks of their respective owners. The Publisher is not associated with any product or vendor mentioned in this book. This publication is designed to provide accurate and authoritative information in regard to the subject matter covered. It is sold on the understanding that the Publisher is not engaged in rendering professional services. If professional advice or other expert assistance is required, the services of a competent professional should be sought.

Limit of Liability/Disclaimer of Warranty: While the publisher and author have used their best efforts in preparing this book, they make no representations or warranties with respect to the accuracy or completeness of the contents of this book and specifically disclaim any implied warranties of merchantability or fitness for a particular purpose. It is sold on the understanding that the publisher is not engaged in rendering professional services and neither the publisher nor the author shall be liable for damages arising herefrom. If professional advice or other expert assistance is required, the services of a competent professional should be sought.

#### Library of Congress Cataloging-in-Publication Data

Names: Omura, Y. (Yasuhisa), author. | Mallik, Abhijit, author. | Matsuo, N. (Naoto), author. Title: MOS devices for low-voltage and low-energy applications / Yasuhisa Omura, Abhijit Mallik, and Naoto Matsuo. Description: Singapore ; Hoboken, NJ : John Wiley & Sons, 2017. | Includes bibliographical references and index. Identifiers: LCCN 2016026240 | ISBN 9781119107354 (cloth) | ISBN 9781119107385 (epub) Subjects: LCSH: Metal oxide semiconductors. | Metal oxide semiconductor field-effect transistors. |

Low voltage integrated circuits. | Low voltage systems–Industrial applications. Classification: LCC TK7871.99.M44 O473 2017 | DDC 621.3815/284–dc23

LC record available at https://lccn.loc.gov/2016026240

Set in 10/12pt Times by SPi Global, Pondicherry, India

 $10 \quad 9 \quad 8 \quad 7 \quad 6 \quad 5 \quad 4 \quad 3 \quad 2 \quad 1$ 

## Contents

Pr	eface	xv
A	knowledgments	xvi
Pa	rt I INTRODUCTION TO LOW-VOLTAGE AND LOW-ENERGY DEVICES	1
1	Why Are Low-Voltage and Low-Energy Devices Desired? References	<b>3</b> 4
2	History of Low-Voltage and Low-Power Devices	5
	2.1 Scaling Scheme and Low-Voltage Requests	5
	2.2 Silicon-on-Insulator Devices and Real History	8
	References	10
3	Performance Prospects of Subthreshold Logic Circuits	12
	3.1 Introduction	12
	3.2 Subthreshold Logic and its Issues	12
	3.3 Is Subthreshold Logic the Best Solution?	13
	References	13
Pa	rt II SUMMARY OF PHYSICS OF MODERN SEMICONDUCTOR DEVICES	15
4	Overview	17
	References	18
5	Bulk MOSFET	19
	5.1 Theoretical Basis of Bulk MOSFET Operation	19
	5.2 Subthreshold Characteristics: "OFF State"	19
	5.2.1 Fundamental Theory	19

		5.2.2	Influence of BTBT Current	23
		5.2.3	Points to Be Remarked	24
	5.3	Post-7	Threshold Characteristics: "ON State"	24
		5.3.1	Fundamental Theory	24
		5.3.2	Self-Heating Effects	26
		5.3.3	Parasitic Bipolar Effects	27
	5.4	Comp	rehensive Summary of Short-Channel Effects	27
	Refe	erences		28
6	SOI	MOSE	EL	29
	6.1	Partia	lly Depleted Silicon-on-Insulator Metal Oxide Semiconductor	
		Field-	Effect Transistors	29
	6.2	Fully	Depleted (FD) SOI MOSFET	30
		6.2.1	Subthreshold Characteristics	30
		6.2.2	Post-Threshold Characteristics	36
		6.2.3	Comprehensive Summary of Short-Channel Effects	41
	6.3	Accur	nulation-Mode (AM) SOI MOSFET	41
		6.3.1	Aspects of Device Structure	41
		6.3.2	Subthreshold Characteristics	42
		6.3.3	Drain Current Component $(I)$ -Body Current $(I_{D,body})$	43
		6.3.4	Drain Current Component (II)–Surface Accumulation	
			Layer Current $(I_{D,acc})$	45
	<i>.</i> .	6.3.5	Optional Discussions on the Accumulation Mode SOI MOSFET	45
	6.4	FinFE	T and Triple-Gate FET	46
		6.4.1	Introduction	46
		6.4.2	Device Structures and Simulations	46
		6.4.3	Results and Discussion	47
		6.4.4	Summary	49
	6.5	Gate-a	all-Around MOSFET	50
	Refe	erences		51
7	Tun	nel Fiel	ld-Effect Transistors (TFETs)	53
	7.1	Overv		53
	1.2	Mode	I of Double-Gate Lateral Tunnel FET and Device Performance	50
		Perspe		53
		7.2.1	Introduction	55
		7.2.2	Device Modeling	54
		7.2.3	Numerical Calculation Results and Discussion	01
	7 2	7.2.4 Mada	Summary	03
	1.5		I of vertical runnel FET and Aspects of its Characteristics	03 65
		7.3.1	Introduction Device Structure and Model Concept	65
		7.3.2	Device Structure and Model Concept	60
		1.3.3 7 2 1	Consideration of the Impact of Turnel Dimensionality on Duivability	09 70
		7.5.4	Consideration of the Impact of Tunnet Dimensionality on Drivability	12 75
	74	/.3.3	Summary	13 76
	7.4 Daf	Apper	iuix integration of Eqs. (7.14)–(7.10)	/0 70
	Keit	rences		/8

Par	t III	POTENTIAL OF CONVENTIONAL BULK MOSFETS	81
8	Perf Sub	ormance Evaluation of Analog Circuits with Deep micrometer MOSFETs in the Subthreshold Regime	
	of O	peration	83
	8.1	Introduction	83
	8.2	Subthreshold Operation and Device Simulation	84
	8.3	Model Description	85
	8.4	Results	86
	8.5	Summary	90
	Refe	rences	90
9	Imp	act of Halo Doping on the Subthreshold Performance of	
	Deej	p-Submicrometer CMOS Devices and Circuits for Ultralow	01
	POW 0.1	er Analog/Mixed-Signal Applications	<b>91</b>
	9.1	Device Structures and Simulation	91
	9.2	Subthrashold Operation	92
	9.5 Q A	Device Optimization for Subthreshold Analog Operation	93
	9.4	Subthreshold Analog Circuit Performance	93
	9.6	CMOS Amplifiers with Large Geometry Devices	105
	97	Summary	105
	Refe	rences	100
10	Stud	ly of the Subthreshold Performance and the Effect of	
	Cha	nnel Engineering on Deep Submicron Single-Stage	
	CM	OS Amplifiers	108
	10.1	Introduction	108
	10.2	Circuit Description	108
	10.3	Device Structure and Simulation	110
	10.4	Results and Discussion	110
	10.5	PTAT as a Temperature Sensor	116
	10.6	Summary	116
	Refe	rences	116
11	Sub	threshold Performance of Dual-Material Gate CMOS	
	Devi	ces and Circuits for Ultralow Power Analog/	
	Mix	ed-Signal Applications	117
	11.1	Introduction	117
	11.2	Device Structure and Simulation	118
	11.3	Kesuits and Discussion	120
	11.4 D-f	Summary	126
	кете	Tences	127
12	Perf	ormance Prospect of Low-Power Bulk MOSFETs	128
	Refe	rence	129

Par	t IV	POTEN	ITIAL OF FULLY-DEPLETED SOI MOSFETS	131
13	Dem	and for ]	High-Performance SOI Devices	133
14	4 Demonstration of 100 nm Gate SOI CMOS with a Thin Buried Oxide Layer			
	and	its Impao	ct on Device Technology	134
	14.1	Introdu	ction	134
	14.2	Device	Design Concept for 100 nm Gate SOI CMOS	134
	14.3	Device	Fabrication	136
	14.4	Perform	nance of 100-nm- and 85-nm Gate Devices	137
		14.4.1	Threshold and Subthreshold Characteristics	137
		14.4.2	Drain Current $(I_D)$ -Drain Voltage $(V_D)$ and $I_D$ -Gate Voltage $(V_G)$	120
		1442	Characteristics of 100-nm-Gate MOSFET/SIMOX	138
		14.4.3	$I_D - V_D$ and $I_D - V_G$ Characteristics of 85-nm-Gate	140
		1 4 4 4		142
	145	14.4.4 Diaguag	Switching Performance	142
	14.3	1451	JUII Threshold Voltago Palanoo in Ultrathin CMOS/SOI Devices	142
	146	14.J.1 Summo	Threshold voltage Balance in Olirainin CMOS/SOT Devices	142
	Pofo	Summa	1 ý	1/14
	Refe	lences		145
15	Disc Sub-	ussion or 50 nm C Imon	1 Design Feasibility and Prospect of High-Performance Thannel Single-Gate SOI MOSFET Based on the ITRS	147
	15 1	Introdu	ction	147
	15.1	Device	Structure and Simulations	147
	15.2	Propose	ed Model for Minimum Channel Length	140
	15.5	1531	Minimum Channel Length Model Constructed using Extract A	149
		15.3.1	Minimum Channel Length Model Constructed using Extract R	150
	154	Perform	nance Prospects of Scaled SOI MOSEETs	150
	15.1	1541	Dynamic Operation Characteristics of Scaled SG SOI MOSFETs	152
		15.4.2	Tradeoff and Optimization of Standby Power Consumption	102
		101112	and Dynamic Operation	157
	15.5	Summa	ďV	162
	Refe	rences		162
16	Perf	ormance	Prospects of Fully Depleted SOI MOSFET-Based Diodes	
	App	lied to Sc	chenkel Circuits for RF-ID Chips	164
	16.1	Introdu	ction	164
	16.2	Remain	ing Issues with Conventional Schenkel Circuits and an Advanced	
		Proposa	al	165
	16.3	Simulat	tion-Based Consideration of RF Performance of SOI-QD	172
	16.4	Summa	ſŗy	176
	16.5	Append	lix: A Simulation Model for Minority Carrier Lifetime	177
	16.6	Append	lix: Design Guideline for SOI-QDs	177
	Refe	rences		178

MOSFET					
17.1 Introduction	180				
17.2 Simulations	181				
17.3 Results and Discussion	183				
17.3.1 DC Characteristics and Switching Performance: Device A	183				
17.3.2 RF Analog Characteristics: Device A	184				
17.3.3 Impact of High-к Gate Dielectric on Performance of					
USU SOI MOSFET Devices: Devices B and C	185				
17.3.4 Impact of Simulation Model on Simulation Results	189				
17.4 Summary	192				
References	192				
18 Practical Source/Drain Diffusion and Body Doping Layouts for					
High-Performance and Low-Energy Triple-Gate SOI MOSFETs	194				
18.1 Introduction	194				
18.2 Device Structures and Simulation Model	195				
18.3 Results and Discussion	196				
18.3.1 Impact of S/D-Underlying Layer on $I_{out}$ , $I_{out}$ , and					
Subthreshold Swing	196				
18.3.2 Tradeoff of Short-Channel Effects and Drivability	196				
18.4 Summary	201				
References	201				
19 Gate Field Engineering and Source/Drain Diffusion Engineering for					
High-Performance Si Wire Gate-All-Around MOSFET and Low-Power					
Strategy in a Sub-30 nm-Channel Regime	203				
19.1 Introduction	203				
19.2 Device Structures Assumed and Physical Parameters	204				
19.3 Simulation Results and Discussion	206				
19.3.1 Performance of Sub-30 nm-Channel Devices and					
Aspects of Device Characteristics	206				
19.3.2 Impact of Cross-Section of Si Wire on Short-Channel					
Effects and Drivability	212				
19.3.3 Minimizing Standby Power Consumption of GAA					
<i>SOI MOSFET</i>	216				
19.3.4 Prospective Switching Speed Performance of GAA SOI MOSFE	T 217				
19.3.5 Parasitic Resistance Issues of GAA Wire MOSFETs	218				
19.3.6 Proposal for Possible GAA Wire MOSFET Structure	220				
19.4 Summary	221				
19.5 Appendix: Brief Description of Physical Models in Simulations	221				
References	225				
20 Impact of Local High-ĸ Insulator on Drivability and Standby					
Dower of Cate All Around SOI MOSEET	228				
I UWEL OF GARE-AIT-ATOUND SOLENUSF F. I					
20.1 Introduction	228				

	20.3	Results and Discussion	230
		20.3.1 Device Characteristics of GAA Devices	
		with Graded-Profile Junctions	230
		20.3.2 Device Characteristics of GAA Devices with Abrupt Junctions	235
		20.3.3 Behaviors of Drivability and Off-Current	237
		20.3.4 Dynamic Performance of Devices with Graded-Profile Junctions	239
	20.4	Summary	239
	Refer	rences	240
Par	tV ]	POTENTIAL OF PARTIALLY DEPLETED SOI MOSFETS	241
21	Pron	osal for Cross-Current Tetrode (XCT) SOI MOSFETs: A 60 dB	
41	Sing	e-Stage CMOS Amplifier Using High-Gain Cross-Current	
	Tetro	MoSFFT/SIMOX	243
	21.1	Introduction	243
	21.1 21.2	Device Eabrication	243
	21.2	Device Characteristics	245
	21.3 21.4	Performance of CMOS Amplifier	245
	21.4	Summary	247
	Z1.J Refer	Summary	249
	Refer		277
22	Devi	ce Model of the XCT-SOI MOSFET and Scaling Scheme	250
	22.1	Introduction	250
	22.2	Device Structure and Assumptions for Modeling	251
		22.2.1 Device Structure and Features of XCT Device	251
		22.2.2 Basic Assumptions for Device Modeling	253
		22.2.3 Derivation of Model Equations	254
	22.3	Results and Discussion	258
		22.3.1 Measured Characteristics of XCT Devices	258
	22.4	Design Guidelines	261
		22.4.1 Drivability Control	261
		22.4.2 Scaling Issues	262
		22.4.3 Potentiality of Low-Energy Operation of XCT CMOS Devices	265
	22.5	Summary	267
	22.6	Appendix: Calculation of MOSFET Channel Current	267
	22.7	Appendix: Basic Condition for Drivability Control	271
	Refer	rences	271
23	Low	Power Multivoltage Reference Circuit Using XCT-SOI MOSFET	274
	23.1	Introduction	274
	23.2	Device Structure and Assumptions for Simulations	274
		23.2.1 Device Structure and Features	274
		23.2.2 Assumptions for Simulations	277
	23.3	Proposal for Voltage Reference Circuits and Simulation Results	278
		23.3.1 Two-Reference Voltage Circuit	278
		23.3.2 Three-Reference Voltage Circuit	283
	23.4	Summary	283
	Refer	rences	284

24	Low	-Energy Operation Mechanisms for XCT-SOI CMOS Devices:		
	Prospects for a Sub-20 nm Regime 24.1 Introduction			
	24.2	Device Structure and Assumptions for Modeling	286	
	24.3	Circuit Simulation Results of SOI CMOS and XCT-SOI CMOS	288	
	24.4	Further Scaling Potential of XCT-SOI MOSFET	291	
	24.5	Performance Expected from the Scaled XCT-SOI MOSFET	292	
	24.6	Summary	296	
	Refe	rences	296	
Par	t VI	QUANTUM EFFECTS AND APPLICATIONS – 1	297	
25	Over	rview	299	
	Refe	rences	299	
26	Si R	esonant Tunneling MOS Transistor	301	
	26.1	Introduction	301	
	26.2	Configuration of SRTMOST	302	
		26.2.1 Structure and Electrostatic Potential	302	
		26.2.2 Operation Principle and Subthreshold Characteristics	304	
	26.3	Device Performance of SRTMOST	307	
		26.3.1 Transistor Characteristics of SRTMOST	307	
		26.3.2 Logic Circuit Using SRTMOST	310	
	26.4	Summary	312	
	Refe	rences	312	
27	Tuni	neling Dielectric Thin-Film Transistor	314	
	27.1	Introduction	314	
	27.2	Fundamental Device Structure	315	
	27.3	Experiment	315	
		27.3.1 Experimental Method	315	
		27.3.2 Calculation Method	317	
	27.4	Results and Discussion	320	
		27.4.1 Evaluation of $SiN_x$ Film	320	
		27.4.2 Characteristics of the TDTFT	320	
		27.4.3 TFT Performance at Low Temperatures	324	
		27.4.4 TFT Performance at High Temperatures	324	
		27.4.5 Suppression of the Hump Effect by the TDTFT	330	
	27.5	Summary	336	
	Refe	rences	336	
28	Prop	oosal for a Tunnel-Barrier Junction (TBJ) MOSFET	339	
	28.1	Introduction	339	
	28.2	Device Structure and Model	339	
	28.3	Calculation Results	340	
	28.4	Summary	343	
	Refe	rences	343	

29	Perfo	ormance	Prediction of SOI Tunneling-Barrier-	214
	<b>June</b>	Introdu	SFEI	244
	29.1	Simula	tion Model	244
	29.2	Simula	tion Results and Discussion	240
	29.5	20.2.1	Lion Results and Discussion	249
		29.3.1	Fundamental Properties of IBJ MOSFEI	249
	20.4	29.3.2 Summer	Optimization of Device Parameters and Materials	249
	29.4 Refei	rences	u y	357
20	DI	• •		
30	Phys Perfo	ics-Base	d Model for TBJ-MOSFETs and High-Frequency Prospects	358
	30.1	Introdu	ction	358
	30.2	Device	Structure and Device Model for Simulations	350
	30.2	Simula	tion Results and Discussion	360
	50.5	30 3 1	Current Drivability	361
		30.3.2	Threshold Voltage Issue	362
		30.3.3	Subthreshold Characteristics	363
		30.3.4	Radio-Frequency Characteristics	363
	30.4	Summa	new requercy characteristics	365
	Refe	rences	,	365
31		Power H	Ligh-Temperature-Operation-Tolerant (HTOT)	2/5
	SOL	MOSFE	T	367
	31.1	Introdu	ction	367
	31.2	Device	Structure and Simulations	368
	31.3	Results	and Discussion	371
		31.3.1	Room-Temperature Characteristics	371
		31.3.2	High-Temperature Characteristics	373
	31.4	Summa	ary	377
	Refe	rences		379
Par	t VII	QUAN	TUM EFFECTS AND APPLICATIONS – 2	381
32	Over	view of '	Tunnel Field-Effect Transistor	383
	Refe	rences		385
33	Impa	act of a S	pacer Dielectric and a Gate Overlap/Underlap on the Device	
	Perfo	ormance	of a Tunnel Field-Effect Transistor	386
	33.1	Introdu	ction	386
	33.2	33.2 Device Structure and Simulation		387
	33.3	Results	and Discussion	387
		33.3.1	Effects of Variation in the Spacer Dielectric Constant	387
		33.3.2	Effects of Variation in the Spacer Width	391
		33.3.3	Effects of Variation in the Source Doping Concentration	392

		33.3.4	Effects of a Gate-Source Overlap	394
		33.3.5	Effects of a Gate-Channel Underlap	394
	33.4	Summa	ıry	397
	Refer	ences		397
34	The l	impact o	f a Fringing Field on the Device Performance of a	
	P-Ch	annel Tu	nnel Field-Effect Transistor with a High-κ Gate Dielectric	399
	34.1	Introdu	ction	399
	34.2	Device	Structure and Simulation	399
	34.3	Results	and Discussion	400
		34.3.1	Effects of Variation in the Gate Dielectric Constant	400
		34.3.2	Effects of Variation in the Spacer Dielectric Constant	408
	34.4	Summa	ıry	410
	Refer	ences		410
35	Impa	ct of a S	pacer-Drain Overlap on the Characteristics of a	
	Silico	n Tunne	el Field-Effect Transistor Based on Vertical Tunneling	412
	35.1	Introdu	ction	412
	35.2	Device	Structure and Process Steps	413
	35.3	Simula	tion Setup	414
	35.4	Results	and Discussion	416
		35.4.1	Impact of Variation in the Spacer-Drain Overlap	416
		35.4.2	Influence of Drain on the Device Characteristics	424
		35.4.3	Impact of Scaling	426
	35.5	Summa	ıry	429
	Refer	ences		430
36	Gate	on-Geri	nanium Source Tunnel Field-Effect Transistor	
	Enab	ling Sub	-0.5-V Operation	431
	36.1	Introdu	ction	431
	36.2	Propose	ed Device Structure	431
	36.3	Simula	tion Setup	432
	36.4	Results	and Discussion	434
		36.4.1	Device Characteristics	434
		36.4.2	Effects of Different Structural Parameters	435
		36.4.3	Optimization of Different Structural Parameters	436
	36.5	Summa	ſſŸ	445
	Refer	ences		445
Par	t VIII	PROS	PECTS OF LOW-ENERGY DEVICE TECHNOLOLGY	
		AND A	APPLICATIONS	447
37	Perfo	rmance	Comparison of Modern Devices	449
	Kefer	ences		450

38	Emerging Device Technology and the Future of MOSFET	452
	38.1 Studies to Realize High-Performance MOSFETs based on	
	Unconventional Materials	452
	38.2 Challenging Studies to Realize High-Performance MOSFETs based	
	on the Nonconventional Doctrine	453
	References	454
39	How Devices Are and Should Be Applied to Circuits	456
	39.1 Past Approach	456
	39.2 Latest Studies	456
	References	457
40	Prospects for Low-Energy Device Technology and Applications	458
	References	459
Bib	liography	460
Ind	lex	463

### Preface

The twin goals of low-voltage operation and low power consumption have been pursued for 40 years, since the adoption of the scaling law. In the 1970s, however, the electronics industry did not pay much attention to the scaling law, despite its advantages, because nobody imagined at that time that the industry would grow so rapidly or that the global social infrastructure would be so thoroughly altered by the Internet.

Since the final decade of the twentieth century, the limitations of petroleum-related chemicals and the threat of global warming have compelled industry leaders and scientists to make serious efforts to find solutions. Population pressure is negatively impacting energy resources and global warming, giving the situation particular urgency.

Against this background, many kinds of monitoring technologies using sensors are being developed. However, the power consumption of such products is very high and high-power batteries are needed as a result.

We, the authors, are interested in the development of low-voltage and low-power semiconductor devices to contribute to the energy efficiency of electronic products. In this book we introduce the concept of "low energy" in discussing the above issues. The meaning of "low energy" is described in the following chapters in detail.

We hope that this book will be helpful in developing low-energy device technologies for the electronics industry and the world.

Yasuhisa Omura, Osaka, Japan Abhijit Mallik, Kolkata, India Naoto Matsuo, Himeji, Japan

### Acknowledgments

The first editor, Professor Yasuhisa Omura, wishes to express his sincere thanks to Dr. Katsutoshi Izumi (the former NTT laboratory director and a professor at Osaka Prefecture University) for his warm support for this study when Dr. Izumi was with NTT Laboratories. He also thanks Ms. Yu Azuma Yoshioka and Mr. Yoshimasa Yoshioka (Graduate School of Engineering, Kansai University; presently with Panasonic, Japan), Mr. Yoshio Mimura (Graduate School of Engineering, Kansai University; presently with Renesas Electronics, Japan), Mr. Daiki Sato (Graduate School of Engineering, Kansai University; presently with Panasonic, Japan), Mr. Shunsuke Nakano (Graduate School of Engineering, Kansai University; presently with Renesas Electronics, Japan), Mr. Osanori Hayashi (Graduate School of Engineering, Kansai University; presently with Roam, Japan), Mr. Hidehiko Nakajima (Graduate School of Engineering, Kansai University; presently with Canon, Japan), Dr. Kenji Komiya (Graduate School of Engineering, Kansai University; presently with Denso, Japan), and Mr. Daishi Ino (Graduate School of Engineering, Kansai University; presently Alps Tech., Japan) for their documentation of experiments, device simulations, and circuit simulations. He gives his special thanks to Dr. Hirobumi Watanabe and Mr. Hidenori Kato (Ricoh, Japan) for the fabrication of XCT SOI devices.

Professor Omura expresses his deep appreciation to Mr. Mike Blackburn (TECH-WRITE, Japan) for his continued guidance in English communication over the past 25 years. He also expresses his gratitude to his family members – wife Kikuyo, son's family, and daughter's family – for their various metal supports.

The second editor, Abhijit Mallik, would like to acknowledge his research collaborator and the first editor, Professor Yasuhisa Omura, who encouraged and convinced him to be a coeditor of this book. Without his tireless efforts, this book would not exist. He would also like to acknowledge the benefit he has gained from the years of collaboration and interaction with Professor V. Ramgopal Rao (Indian Institute of Technology, Mumbai, India), Prof. Chandan Sarkar (Jadavpur University, Kolkata, India), and Prof. Anupam Karmakar (University of Calcutta, Kolkata, India). He expresses his thanks to his graduate students, Dr. Saurav Chakraborty (presently with Tyfone Communications Development (India) Pvt. Ltd., Bangalore, India), Professor Srimanta Baishya (currently with the National Institute of Technology, Silchar, India), Dr. Avik Chattopadhyay (currently with the Birla Institute of Technology and Science, Pilani, India), Ms. Shilpi Guin (presently a research scholar with the University of Calcutta, Kolkata, India), and Mr. Asish Debnath, who helped to bring this work to its present form over the years. He is also grateful to his family members – mother Muktakeshi Mallik, wife Arpita Mallik, son Abhishek, and daughter Annika – for their constant encouragement and patience during the entire process. Finally, he expresses his gratitude to his late father Raghunath Mallik, whose memory helped him through the process of writing.

The third editor of this book, Naoto Matsuo, wishes to thank sincerely Yasuhisa Omura, and also Dr. Shin Yokoyama, Hiroshima University, and Dr. Hiroki Hamada, Director of the Research Department of Sanyo Electric Co., presently at the Kinki University, for their useful discussions. Measurement of the electrical characteristics of the tunneling dielectric thin-film transistor (TDTFT) and conventional thin-film transistor (TFT) at low and high temperatures was performed at the Omura Laboratory, Kansai University. The TDTFT and the conventional TFT were fabricated at Research Institute for Nanodevices and Bio Systems, Hiroshima University, supported by the Nanotechnology Support Project of the Ministry of Education, Culture, Sports, Science and Technology (MEXT), Japan. A part of this study was supported by *Kakenhi* (grants-in-aid) MEXT and by the Ozawa and Yoshikawa Memorial Electronics Research Foundation. Naoto Matsuo also thanks Dr. Akira Heya, associate professor at the University of Hyogo, Dr. Takahiro Kobayashi, Yumex Inc., Japan, Dr. Naoya Kawamoto, Yamaguchi University, Dr. Kensaku Ohkura, Hiroshima University, and the many master's course students of Yamaguchi University and the University of Hyogo, for carrying out experiments and simulations.

He is deeply grateful to Dr. Akio Sasaki, an emeritus professor of Kyoto University and Osaka Electrical and Communication University, and Dr. Hiroyuki Matsunami, an emeritus professor of Kyoto University, for their useful comments and encouragement during the earlier period of this study.

On behalf of the editors, Professor Omura expresses his thanks to Mr. James W. Murphy for his assistance because he warmly accepted the task of examining the book proposal, and to Ms Maggie Zhang, Ms Victoria Taylor and Ms Nivedhitha Elavarasan for their guidance.

Finally, the authors would all like to express their appreciation to the Japan Society of Applied Physics (JSAP), the Institute of Electronics, Information, and Communication Engineers (IEICE), the Electrochemical Society (ECS), the Institute of Electrical and Electronics Engineers (IEEE), Elsevier Limited, and Springer for their cooperation in granting permission to reproduce original papers or figures.

# Part I INTRODUCTION TO LOW-VOLTAGE AND LOW-ENERGY DEVICES

## 1

## Why Are Low-Voltage and Low-Energy Devices Desired?

The original scaling rule [1] indicated that the dissipation power density (W/cm<sup>2</sup>) of an integrated circuit is not changed by scaling [1, 2]. However, this guideline is only really applicable to DRAM devices. In most integrated circuits, the supply voltage is not scaled according to the designer's intent, and devices have faced negative impacts, such as hot-carrier phenomena [3] and negative bias temperature instability (NBTI) phenomena [4], due to high supply voltages [5]. In the twentieth century, central processing unit (CPU) revealed dramatic advances in device performance (high-speed signal processing with increases in data bit length), and the guideline seemed to be ignored (see http://www.depi.itch.edu.mx/apacheco/asm/Intel\_cpus.htm, accessed May 18, 2016).

However, in the 1990s, CPU designers noticed the limitations of CPU cooling efficiency, which triggered an urgent and ongoing discussion of low-power device technology. The following possible solutions have been proposed:

- the introduction of a silicon-on-insulator integrated circuit (SOI IC) strategy based on advanced substrate technology [6];
- a multicore strategy [7];
- a low-voltage strategy [8].

These major strategic proposals have led the worldwide electronics industry to the Internet of Things.

Business opportunities based on information technology have increased in the real world without taking account of the issues raised by technologies such as cloud computing [9] and datacenter construction (see http://www.datacenterknowledge.com/,

Yasuhisa Omura, Abhijit Mallik, and Naoto Matsuo.

MOS Devices for Low-Voltage and Low-Energy Applications, First Edition.

<sup>© 2017</sup> John Wiley & Sons Singapore Pte. Ltd. Published 2017 by John Wiley & Sons Singapore Pte. Ltd.

accessed May 18, 2016), which have rapidly increased global energy consumption [10]. We must propose viable and innovative ideas on semiconductor device technologies to suppress such global-warming factors.

Information technology has widened perspectives on improving the quality of our future social life. Many companies are creating highly desirable products in the field of sensing technology, such as house monitoring (temperature, humidity, air pollution, fire, human health, security), office monitoring (temperature, humidity, air pollution, fire, security), traffic monitoring (for aspects such as car speed, traffic jams, and accidents), agriculture monitoring (for temperature, humidity, air pollution, rain, wind, lighting, storms), space monitoring (moon, sun, stars, meteorites, and other astronomical phenomena), defense monitoring, and so on. Many of these products use dry batteries or solar power/batteries for 24-hour monitoring. In the case of portable equipment, large batteries are impractical, which has triggered the development of small batteries with high energy density. This is also applicable to cellular phones and smart phones [11].

In battery-powered sensing devices, the battery volume must be small. This may be achieved by lowering the supply voltage, which in turn reduces the battery energy as it is proportional to the square of the voltage. Hence, it is more important to reduce the dissipation energy than the dissipation power for sensing devices. This will be addressed again later. We must, therefore, contribute to the solution of urgent social problems by proposing low-energy devices and integrated circuits.

### References

- R. H. Dennard, F. H. Gaensslen, H.-N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion implanted MOSFETs with very small physical dimensions," *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 256–268, 1974.
- [2] P. K. Chatterjee, W. R. Hunter, T. C. Holloway, and Y. T. Lin, "The impact of scaling laws on the choice of N-channel or P-channel for MOS VLSI," *IEEE Electron Device Lett.*, vol. EDL-1, pp. 220–223, 1980.
- [3] T. H. Ning, "Hot-electron emission from silicon into silicon dioxide," *Solid-State Electron.*, vol. 21, pp. 273–282, 1978.
- [4] D. K. Schroder and J. A. Babcock, "Negative bias temperature instability: road to cross in deep submicron silicon semiconductor manufacturing," J. Appl. Phys., vol. 94, pp. 1–18, 2003.
- [5] B. Kaczer, R. Degraeve, M. Rasras, K. Van de Mieroop, P. J. Roussel, and G. Groeseneken, "Impact of MOSFET gate oxide breakdown on digital circuit operation and reliability," *IEEE Trans. Electron Devices*, vol. 49, pp. 500–506, 2002.
- [6] M. Canada, C. Akroul, D. Cawlthron, J. Corr, S. Geissler, R. Houle, P. Kartschoke, D. Kramer, P. McCormick, N. Rohrer, G. Salem, and L. Warriner, "Impact of MOSFET Gate Oxide Breakdown on Digital Circuit Operation and Reliability," IEEE Int. Solid State Circ. Conf. (ISSCC), Dig. Tech. Papers, pp. 430–431, 1999.
- [7] T. Chen, R. Raghavan, J. N. Dale, and E. Iwata, "Cell broadband engine architecture and its first implementation A performance view," *IBM J. Res. Dev.*, vol. 51, pp. 559–570, 2007.
- [8] S. Hanson, B. Zhai, K. Bernstein, D. Blaauw, A. Bryant, L. Chang, K. K. Das, W. Haensch, E. J. Nowak, and D. M. Sylvester, "Ultralow-voltage minimum-energy CMOS," *IBM J. Res. Dev.*, vol. 50, pp. 469–490, 2006.
- [9] Meil, P., and Grance, T., "The NIST Definition of Cloud Computing," NIST, 2011.
- [10] G. Fettweis and E. Zimmermann, "ICT Energy Consumption-Trends and Challenges," The 11th Int. Symp. on Wireless Personal Multimedia Communications (WPMC 2008) (Finland, Sept., 2008), Session WG1: W-GREEN 2008 (I), 2008.
- [11] Y. Orikasa, T. Masese, Y. Koyama, T. Mori, M. Hattori, K. Yamamoto, T. Okado, Z.-D. Huang, T. Minato, C. Tassel, J. Kim, Y. Kobayashi, T. Abe, H. Kageyama, and Y. Uchimoto, "High energy density rechargeable magnesium battery using earth-abundant and non-toxic elements," *Sci. Rep.*, vol. 4, Article number: 5622, 2014.

## History of Low-Voltage and Low-Power Devices

### 2.1 Scaling Scheme and Low-Voltage Requests

Dennard *et al.* [1] considered the impact of device scaling on device performance. They assumed the device parameters and voltage parameters shown in Table 2.1 when the so-called "constant-field scaling" method was proposed. They assumed the following expression for the metal oxide semiconductor field-effect transistor (MOSFET) drain current:

$$I_D = \left(\frac{W_G}{L_G}\right) C_{ox} \mu_{eff} \left(V_G - V_{TH} - V_D / 2\right) V_D$$
(2.1)

where  $W_G$  is the gate width,  $L_G$  is the gate length,  $C_{ox}$  is the gate capacitance per unit area,  $\mu_{eff}$  is the carrier mobility,  $V_G$  is the gate voltage,  $V_{TH}$  is the threshold voltage, and  $V_D$  is the drain voltage. Calculation results for the scaling factor (k) are summarized in Table 2.2. They reveal the following features of scaled parameters:

- 1. The electric field in the device and the averaged carrier velocity are static.
- 2. Capacitance components, including the depletion layer capacitance, shrink at the rate of 1/k.
- 3. The carrier density of the inversion layer in the "ON" state does not change.
- 4. Drain current (drift current) decreases at the rate of 1/k.
- 5. Channel resistance does not change.
- 6. Switching delay time/device (intrinsic delay time) decreases at the rate of 1/k.
- 7. The dissipation power/device decreases at the rate of  $1/k^2$ .
- 8. The power-delay product/device shrinks at the rate of  $1/k^3$ .
- 9. The dissipation power of devices/unit area does not change.

Yasuhisa Omura, Abhijit Mallik, and Naoto Matsuo.

MOS Devices for Low-Voltage and Low-Energy Applications, First Edition.

<sup>© 2017</sup> John Wiley & Sons Singapore Pte. Ltd. Published 2017 by John Wiley & Sons Singapore Pte. Ltd.

Parameters	Initial value
$ \begin{array}{c} t_{ox} \\ N_A \\ L_G \\ W_G \\ V_{D'} V_G \end{array} $	100 nm $5 \times 10^{15} \text{ cm}^{-3}$ $5 \ \mu\text{m}$ $5 \ \mu\text{m}$ $20 \ \text{V}$

**Table 2.1** Physical parameters of MOSFET [1].

Parameters	Scaling factor
Circuit performance	
Device dimension $t_{ar}$ , $L_{a}$ , $W_{a}$	1/k
Doping concentration $N_{A}$	k
Voltage V	1/k
Current I	1/k
Capacitance C	1/k
Delay time/circuit VC/I	1/k
Power dissipation/circuit VI	$1/k^{2}$
Power density VI/A	1
Interconnection lines	
Line resistance $R_i$	k
Normalized voltage drop <i>IR</i> ,/V	k
Line response time $R_1/C$	1
Line current density <i>I</i> /A	k

**Table 2.2**Constant field scaling and results [1].

One important feature that attracted attention in the 1970s was 6. but the concept of "constant-field scaling" was not adopted in industry until after the 1980s [2, 3]. As a result, feature 6. was successful, but features 7.–9. were lost.

From the latter half of the 1990s, the semiconductor industry was able to employ lower supply voltages. The popularity of cellular phones created new demands on the semiconductor industry. As cellular phones must be extremely portable, they need a small battery; this strong demand resulted in low-voltage IC designs. In addition, many battery vendors contributed to battery downsizing and battery energy density enhancement.

Lowering the supply voltage accelerates device scaling. However, the scaling trend ignored the original concept proposed by Dennard *et al.* [1]; the dissipation power of integrated circuits (ICs) per unit area was already much higher than the value estimated by the original scaling concept even though the supply voltage was successfully lowered [4]. The surface temperatures of integrated processor circuits are reaching dangerous values (the intrinsic temperature) [5]. Moreover, we now face the negative influence of several physical device parameters on IC performance because they do not follow any scaling rule. The following are typical of the parameters showing such undesirable behavior:

- 1. Electric-field induced mobility degradation.
- 2. Depletion capacitance of poly-Si gate and inversion layer capacitance.

7

- 3. Subthreshold swing.
- 4. Parasitic resistance of devices (gate electrode, source diffusion, drain diffusion, contacts).
- 5. Leakage current (pn junctions, gate insulator).
- 6. Threshold voltage.

Issue 1. can basically be overcome using strain technology [6]. Issue 2. can be addressed by using high- $\kappa$  dielectrics [7], and issue 4. can be improved drastically by the gate-last process [8] and the silicidation process [9]. Issue 6. is aided somewhat by adopting the metal-gate electrode. Issue 5. can be improved by using hetero-junctions and introducing high- $\kappa$  dielectrics. However, issue 3. remains unresolved because there is no agreement on the design methodology that will allow use of subthreshold operation, or on how to design steep swing devices. Subthreshold logic circuits were proposed to realize the ultimate in low-energy operation [10]. In contrast, steep-swing devices, such as tunnel field-effect transistors (TFETs), were proposed in order to lower the supply voltage and to advance the radio frequency performance of MOSFETs [11]. The TFET device technology is still under investigation, and doesn't yet appear to be a reliable solution for future electronics. It is, however, a leading candidate. This book will discuss the above two concerns; that is, useful applications of subthreshold characteristics and the potential of steep-swing devices.

Before discussing individual solutions, we estimate the power consumption and dissipation energy of conventional complementary metal oxide semiconductor (CMOS) devices. Here we assume the following two equations:

Dissipation power density 
$$(W / cm^2) = P_{ON} + P_{OFF}$$
  
=  $r_{ON} f_{clock} \frac{1}{2} C V_D^2 N_{device} + r_{OFF} I_{leak} V_D N_{devices}$  (2.2)

$$Dissipation energy density (J / cm2) = E_{ON} + E_{OFF}$$
$$= T_{one-sec} \left( r_{ON} f_{clock} \frac{1}{2} C V_D^2 N_{device} + r_{OFF} I_{leak} V_D N_{devices} \right)$$
(2.3)

where  $P_{ON}$  denotes the dissipation power density in the "ON" state,  $P_{OFF}$  denotes the dissipation power density in the "OFF" state,  $N_{device}$  denotes the number of devices per unit area,  $r_{ON}$  denotes the fraction of devices working,  $r_{OFF}$  denotes the fraction of devices in standby,  $f_{clock}$  denotes the clock frequency,  $I_{leak}$  denotes the leakage current of the device,  $V_D$  denotes the supply voltage, C denotes the gate capacitance of single CMOS, and  $T_{one-sec}$  denotes the one-second period.

We calculated the dissipation energy of ICs using the equations as shown in Figure 2.1, where we assumed post-1980 device technology. Device parameters assumed in the calculations are summarized in Table 2.3.

Figure 2.1 raises the following key points:

- 1.  $E_{OFF}$  has significantly increased this century;
- 2.  $V_{TH}$  is approaching the thermal voltage;
- 3. the subthreshold swing should be steep.



Figure 2.1 Evolution of performance parameters. It is assumed that  $r_{ON} = 0.5$ , subthreshold swing = 70 mV/dec, and  $W_c/L_c = 5$ .

Years	$L_{G}(\mathrm{nm})$	EOT (nm)	$V_{D}(\mathbf{V})$	$V_{TH}(\mathbf{V})$	$f_{clock}$ (Hz)	N <sub>device</sub> (cm <sup>-2</sup> )
1980	2000	50	5.0	1.0	$5 \times 10^{6}$	$7 \times 10^{4}$
1990	600	20	3.3	0.7	$1 \times 10^{8}$	$1 \times 10^{6}$
2000	200	8.0	2.5	0.5	$1 \times 10^{9}$	$5 \times 10^{6}$
2005	55	2.2	2.0	0.4	$3 \times 10^{9}$	$8 \times 10^{7}$
2010	30	1.4	1.5	0.2	$3 \times 10^{9}$	$3 \times 10^{8}$
2015	24	1.1	1.0	0.15	$3 \times 10^{9}$	$5 \times 10^{8}$

Table 2.3Parameters in simulations.

EOT: equivalent oxide thickness.

The calculation results suggest that we must continuously lower the supply voltage, but also that we will reach its floor (the thermal voltage,  $\sim 26$  mV at 300 K) [12].

### 2.2 Silicon-on-Insulator Devices and Real History

In the 1980s, silicon-on-insulator (SOI) substrate technology emerged and was commercialized. Before the 1980s, silicon-on-sapphire (SOS) substrate technology was the major material for SOI device applications [13]. The SOI substrate was studied in order to develop high-speed switching devices because the silicon-on-sapphire metal oxide semiconductor field-effect transistor (SOS MOSFET) had a much smaller parasitic capacitance beneath the source and drain diffusions than the bulk MOSFET. However, the SOS material had some serious issues, such as the autodoping of Al from the sapphire substrate and high-density defects near the Si/sapphire interface. The Si-based SOI substrate technology basically replaced the SOS substrate technology because the latter's shortcomings could not be ignored by 1990.

Before the 1990s, the electronics industry focused on the signal processing speed of ICs. After the 1990s, however, the industry had to pay attention to IC dissipation power because energy concerns were becoming more pronounced. Accordingly, leading scientists and engineers studied the low-power performance of SOI ICs with low-power dissipation closely [14], and many companies began studies to develop high-performance ICs [15]. Many scientists and engineers, however, remained skeptical about whether sub-100 nm gate silicon-on-insulator complementary metal oxide semiconductor (SOI CMOS) technology was actually suitable for creating the ICs needed in the twenty-first century because no aggressive technical vision had been published. Such negative perceptions were familiar in the electronics industry because nobody predicted the dramatic expansion of worldwide use of mobile phones and tablet PCs. Before specific ICs for mobile phones were developed, the power supply voltage was still high (~3 V). The voltage level was too high to yield a 100 nm gate SOI CMOS with fully depleted mode operation; the parasitic bipolar phenomenon induces the single-transistor latch [16], and many engineers were very skeptical as to the reality of scaled fully depleted silicon-on-insulator metal oxide semiconductor field-effect transistors (SOI MOSFETs). Fortunately, in the latter half of the 1990s, many businessmen began to use cellular phones and notebook PCs, forcing the electronics industry to overcome the historical barrier of power-supply voltage. This breakthrough gave the fully depleted SOI devices a good business opportunity with the result that they are used in many commercial electronics products.

Dr. K. Izumi and his group developed the ITOX-SIMOX (Internal Thermal OXidation-Separation by IMplanted OXygen) substrate [17], which can be applicable to scaled CMOS devices, and one of the editors (Omura) and his colleagues in NTT Laboratories demonstrated the potential of the 100 nm gate SOI CMOS IC with fully depleted components [18]. With the development of the oxygen ion-implanter, commercially viable SIMOX substrates became possible [19], SIMOX substrates were used to fabricate SOI devices and circuits in the laboratories of many companies. After the 1980s, other SOI substrate fabrication technologies, such as ELTRAN<sup>®</sup> and UNIBOND<sup>®</sup>, were also proposed [20–23], and have now entered commercialization. In the twenty-first century, companies that could catch this technology trend are doing well, while those that could not faltered.

Let us consider how we can use the low-power performance of SOI MOSFETs. Intrinsic switching delay time ( $\tau$ ) and dissipation power ( $P_{\alpha N}$ ) of SOI MOSFET are given by

Switching delay time 
$$(\tau / Tr) = (L_G W_G C_{ox} + L_G W_G C_{S,D}) \frac{V_D}{I_D} + C_P \frac{V_D}{I_D}$$
 (2.4)

Dissipation power 
$$(P_{ON} / Tr) = V_D I_D$$
 (2.5)

where  $C_{ox}$  denotes the gate capacitance per unit area,  $C_{s,D}$  denotes the source and drain capacitance per unit area, and  $C_p$  denotes the parasitic capacitance except  $C_{s,D}$ . Energy dissipated by a single switching event ( $\tau P_{ON}$ ) can be estimated as

$$Power \cdot Delay \ product \left( P_{ON} \cdot \tau \ / \ Tr \right) = \left\{ \left( L_G W_G C_{ox} + L_G W_G C_{S,D} \right) + C_P \right\} V_D^2.$$
(2.6)

Estimated dissipation power of IC  $(P_{ON})$  is given by using the clock frequency  $(f_{clock})$ :

$$P_{ON} = N_{device} f_{clock} \left\{ \left( L_G W_G C_{ox} + L_G W_G C_{S,D} \right) + C_P \right\} V_D^2$$

$$\tag{2.7}$$

We must also take account of the standby power of the IC  $(P_{OFF})$ , given by

$$P_{OFF} = N_{device} I_{leak} V_D \tag{2.8}$$

As a result, the overall dissipation power  $(P_{total})$  of the LSI is given by

$$P_{total} = P_{ON} + P_{OFF}$$

$$= N_{device} f_{clock} \left\{ \left( L_G W_G C_{ox} + L_G W_G C_{S,D} \right) + C_P \right\} V_D^2 + N_{devices} I_{leak} V_D$$

$$(2.9)$$

In the above expressions, the terms that are significantly different from the estimated values of the bulk MOSFET are those that include  $C_{s,D}$  and  $C_p$  In SOI CMOS devices, we can predict a reduction in  $I_{leak}$  due to a reduction in effective junction area, suppression of  $I_{leak}$  increases based on better subthreshold swing values, and  $C_p$  reductions due to shrinkage of device isolation area, resulting in the suppression of increases in  $P_{total}$ . However, as the IC designer is always seeking to enhance signal-processing performance,  $P_{ON}$  will increase due to the increase in the value of  $N_{device}f_{clock}$ . When the IC designer lowers the MOSFET threshold voltage to raise the switching speed,  $I_{leak}$  inevitably increases.

Recent  $P_{OFF}$  values are comparable to  $P_{ON}$  due to  $I_{leak}$ . IC designers are suffering from this conundrum. Therefore, one of the primary concerns of this book is how to suppress  $P_{OFF}$  as well as whether we can find applications that do not need high-speed performance.

In Part II, we review the fundamentals of conventional MOSFETs, SOI MOSFETs, and TFETs. This part will help readers to follow easily the discussions in the other parts. In Part III, we discuss how we can use the low-energy performance of bulk MOSFETs and how we can apply such devices to low-energy circuits. In Part IV, we review the low-energy performance potential of fully depleted SOI MOSFETs and introduce examples. In Part V, we address the low-energy performance potential of cross-current tetrode (XCT) SOI MOSFETs, which were proposed to realize extremely low energy circuits. In Part VI, the low-energy potential of quantum-effect devices, proposed by taking account of geometrical aspects, is considered. In Part VII, we discuss comprehensively how we can suppress the energy dissipation by using TFETs, one of the more recent quantum-effect devices. In Part VIII, finally, we briefly compare the performance of various devices and review considerations described in Part III to Part VII. We also address the latest low-energy devices, circuit applications, and future perspectives.

#### References

- R. H. Dennard, F. H. Gaensslen, H.-N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of ion implanted MOSFETs with very small physical dimensions," *IEEE J. Solid-State Circuits*, vol. SC-9, pp. 256–268, 1974.
- [2] P. K. Chatterjee, W. R. Hunter, T. C. Holloway, and Y. T. Lin, "The impact of scaling laws on the choice of N-channel or P-channel for MOS VLSI," *IEEE Electron Device Lett.*, vol. EDL-1, pp. 220–223, 1980.
- [3] T. H. Ning, "Hot-electron emission from silicon into silicon dioxide," *Solid-State Electron.*, vol. 21, pp. 273–282, 1978.
- [4] C. Fiegna, H. Iwai, T. Kimura, S. Nakamura, E. Sangiorgi, and B. Riccò, "Monte Carlo Analysis of Hot Carrier Effects in Ultra Small Geometry MOSFETs," Int. Workshop on VLSI Process and Device Modeling: VPAD (Nara, 1993), pp. 102–103, 1993.
- [5] S. M. Sze and K. K. Ng, "Physics of Semiconductor Devices," 3rd ed. (John Wiley & Sons, Inc., 2007), p. 20 and p. 26.

- [6] Z. Y. Cheng, M. T. Currie, C. W. Leitz, G. Taraschi, E. A. Fitzgerald, J. L. Hoyt, and D. A. Antoniadis, "Electron mobility enhancement in strained-Si n-MOSFETs fabricated on SiGe-on-insulator (SGOI) substrates," *IEEE Electron Device Lett.*, vol. 22, pp. 321–323, 2001.
- [7] V. Misra, G. Lucovsky, and G. Parsons, "Issues in high-k gate stack interfaces," MRS Bull., vol. 27, pp. 212–216, 2001.
- [8] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. McIntyre, P. Moon, J. Neirynck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, and K. Zawadzki, "A 45 nm Logic Technology with High-κ+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193 nm Dry Patterning, and 100% Pb-free Packaging," IEEE IEDM Tech. Dig. (Washington DC, 2007), pp. 247–250, 2007.
- [9] J. Kedzierski, P. Xuan, E. H. Andersonf, J. Bokor, T.-J. King, and C. Hu, "Complementary Silicide Source/Drain Thin-Body MOSFETs for the 20 nm Gate Length Regime," Tech. Dig. IEEE IEDM (San Francisco, 2000) pp. 57–60, 2000.
- [10] S. A. Vitale, P. W. Wyatt, N. Checka, J. Kedzierski, and C. L. Keast, "FESOI process technology for subthreshold-operation ultralow-power electronics," *Proc. IEEE*, vol. 98, pp. 333–342, 2010.
- [11] K. K. Bhuwalka, J. Schulze, and I. Eisele, "Performance enhancement of vertical tunnel field-effect transistor with SiGe in the layer," *Jpn. J. Appl. Phys.*, vol. 43, no. 7A, pp. 4073–4078, 2004.
- [12] R. Landauer, "Irreversibility and heat generation in the computing process," IBM J. Res. Dev., vol. 5, pp. 183–191, 1961.
- [13] J.-P. Colinge, "Silicon-on-Insulator Technology: Materials to VLSI," 3rd ed. (Kluwer Academic Publishers, 2004), pp. 12–13.
- [14] M Itoh, Y. Kawai, S. Ito, K. Yokomizo, Y. Katakura, Y. Fukuda, F. Ichikawa, "Fully Depleted SIMOX SOI Process Technology for Low-Power Digital and RF Device," Proc. 10th Int. Symp. Silicon on Insulator Technology and Devices (The Electrochem. Soc.) (Washington DC, 2001) Vol. 2001-3, pp. 331–336, 2001.
- [15] J.-P. Colinge, "Silicon-on-Insulator Technology: Materials to VLSI," 3rd ed. (Kluwer Academic Publishers, 2004), Chapter 8.
- [16] C.-E. D. Chen, M. Matloubian, R. Sundaresan, B. Mao, C. C. Wei, and G. P. Pollack, "Single-transistor Latch in SOI MOSFETs," *IEEE Electron Device Lett.*, vol. 9, pp. 636–638, 1988.
- [17] S. Nakashima, Y. Omura, and K. Izumi, "A High-Quality SIMOX Wafer and Its Application to Ultrathin-Film MOSFETs," Proc. 5th Int. Symp. on SOI Technol. Dev. (The Electrochem. Soc., 1992) Vol. 92–13, pp. 358–367, 1992.
- [18] Y. Omura, S. Nakashima, K. Izumi, and T. Ishii, "0.1-µm-Gate, Ultrathin-Film CMOS Devices Using SIMOX Substrate with 80-nm-Thick Buried Oxide Layer," 1991 IEEE Int. Electron Devices Meeting, Tech. Dig., pp. 675–678, 1991.
- [19] K. Izumi, Y. Omura, and S. Nakashima, "Promotion of practical SIMOX technology by the development of a 100 mA-class high-current oxygen implanter," *Electron. Lett*, vol. 22, no. 15, pp. 775–777, 1986.
- [20] T. Yonehara, K. Sakaguchi, and N. Sato, "Epitaxial layer transfer by bond and etch back of porous Si," Appl. Phys. Lett., vol. 64, pp. 2108–2110, 1994.
- [21] T. Yonehara and K. Sakaguchi, "ELTRAN<sup>®</sup>; novel SOI wafer technology," Jpn. Soc. Appl. Phys. Int., no. 4, pp. 10–16, 2001.
- [22] M. Bruel, "Application of hydrogen ion beams to silicon on insulator. Material technology," Nucl. Instrum. Methods Phys. Res., Sect. B, vol. 108, pp. 313–319, 1996.
- [23] G., Celler "Smart Cut<sup>®</sup>, A guide to the technology, the process, the products," SOITEC, Press Release, July 1, 2003.

## Performance Prospects of Subthreshold Logic Circuits

### 3.1 Introduction

The possibility of lowering the dissipation energy is addressed for the following conventional device technologies:

- multithreshold circuits [1];
- power management [2];
- subthreshold logic [3].

In a multithreshold circuit, designers can assume that different circuit blocks can have different threshold voltages. They can set low threshold voltages for high-speed circuit blocks and high threshold voltages for low-power circuit blocks. This technique is widely applied to commercial integrated circuits (ICs). In the case of power management, the power supply is switched in individual circuit blocks; this is a more recent technique, used most often in mobile electronics. In some cases the signal-processing speed might be degraded. In the case of sub-threshold logic, conventional device technology is assumed but the supply voltage is lowered to the threshold voltage or much less. The logic circuit works in the subthreshold current range. In the last century this design approach was applied to control circuits in wrist watches [4].

### 3.2 Subthreshold Logic and its Issues

As described in the previous section, circuit designers initially used multithreshold devices and power management to reduce the dissipation power of ICs. These ideas are not innovative, as they are mere extensions of conventional techniques. Reducing dissipation power by lowering

Yasuhisa Omura, Abhijit Mallik, and Naoto Matsuo.

MOS Devices for Low-Voltage and Low-Energy Applications, First Edition.

<sup>© 2017</sup> John Wiley & Sons Singapore Pte. Ltd. Published 2017 by John Wiley & Sons Singapore Pte. Ltd.

the supply voltage is also a conventional design guideline, where metal oxide semiconductor field-effect transistors (MOSFETs) are used in the conventional manner in the circuit.

On the other hand, the subthreshold logic and near-subthreshold logic approaches are quite different from the design idea of focusing on "ON" state performance. Circuit designers are now paying close attention to the quasi-"OFF" state. Rather than using the high impedance of the device, they target extremely low currents for logic circuits.

When we apply the subthreshold current of the MOSFET to low-power circuits, we must be careful of the noise issue, the variability of characteristics, and nonlinearity of *I-V* characteristics. Verma *et al.* recently addressed these points in detail [5].

#### **3.3** Is Subthreshold Logic the Best Solution?

Low-power logic circuits, like the subthreshold logic circuits described in the previous section, are now commercialized as ICs for wrist watches [6]; such circuits were the concern of a small group of engineers and the design methodology was not familiar to most engineers. There was skepticism regarding whether a design technique based on subthreshold logic circuits would be utilized frequently.

In order to change these negative impressions, one of the editors (Omura) proposed the cross-current tetrode-silicon-on-insulator metal oxide semiconductor field-effect transistor (XCT-SOI MOSFET) [7, 8]. One of its advantages is the fact that we can basically design the required circuits by applying conventional design methodology in terms of supply voltage and device layout patterns. We can reduce the dissipation power by two orders when the "source potential floating effect" is significant. The most important point in the device design is that we can simply assume the stable saturation region of the drain current despite a very low drain current comparable to the subthreshold level. Details of device characteristics and aspects are described in Part V. We therefore still have many choices for reducing dissipation energy in various circuit applications.

#### References

- T. Douseki, J. Yamada, and H. Kyuragi, "Ultra Low-Power CMOS/SOI LSI Design for Future Mobile Systems," Dig. of Technical Papers, Int. Symp. on VLSI Circuits, June 2002, pp. 6–9, 2002.
- [2] S. Mutoh, T. Douseki, Y. Matsuya, T. Aoki, S. Shigematsu, and J. Yamada, "1-V power supply high-speed digital circuit technology with multithreshold-voltage CMOS," *IEEE J. Solid-State Circuits*, vol. 30, pp. 847–854, 1995.
- [3] S. A. Vitale, P. W. Wyatt, N. Checka, J. Kedzierski, and C. L. Keast, "FESOI process technology for subthresholdoperation ultralow-power electronics," *Proc. IEEE*, vol. 98, pp. 333–342, 2010.
- [4] E. Vittoz, B. Gerber, and F. Leuenberger, "Silicon-gate CMOS frequency divider for the electronic wrist watch," *IEEE J. Solid-State Circuits*, vol. 7, pp. 100–104, 1972.
- [5] N. Verma, J. Kwong, and A. P. Chandrakasan, "Nanometer MOSFET variation in minimum energy subthreshold circuits," *IEEE Trans. Electron Devices*, vol. 55, pp. 163–174, 2008.
- [6] C. Piguet, "Low-Power CMOS Circuits –Technology, Logic Design and CAD Tools," (CRC Press, 2006), Chapter 1.
- [7] Y. Omura, Y. Azuma, Y. Yoshioka, K. Fukuchi, and D. Ino, "Proposal of preliminary device model and scaling scheme of cross-current tetrode silicon-on-insulator metal-oxide-semiconductor field-effect transistor aiming at low-energy circuit applications," *Solid-State Electron.*, vol. 64, pp. 18–27, 2011.
- [8] Y. Omura and D. Sato, "Mechanisms of low-energy operation of XCT-SOI CMOS devices Prospect of sub-20nm regime," J. Low Power Electron. Appl., vol. 4, pp. 14–25, 2014.

# Part II SUMMARY OF PHYSICS OF MODERN SEMICONDUCTOR DEVICES

## 4

### Overview

This part describes the fundamentals of metal oxide semiconductor (MOS) device physics. First, we describe the physics of bulk metal oxide semiconductor field-effect transistors (MOSFETs). Then, some important physics related to silicon-on-insulator metal oxide semiconductor field-effect transistors (SOI MOSFETs) (partially depleted SOI MOSFET, fully depleted SOI MOSFET, FinFET, Triple-gate FET, gate-all-around MOSFET) are introduced, followed by the theoretical basis of tunnel field-effect transistors (TFETs).

The accumulation condition, the depletion condition, and the inversion condition in bulk MOSFET are explained. Threshold voltage and subthreshold swing are also explained as important parameters of MOSFET [1, 2]. In SOI MOSFETs, aspects of partially depleted (PD) SOI MOSFETs and fully depleted (FD) SOI MOSFETs are outlined [3, 4]. The reasons why FinFET, Triple-gate FET, and Gate-All-Around (GAA) MOSFET are superior to the PD and FD SOI MOSFETs are discussed [5, 6], and their details are described in the following parts. Finally, we discuss the physics of TFETs [7].

It is obvious that we must minimize the subthreshold swing (SS) value of the MOS device in designing device parameters for low-power applications. However, there is still some controversy regarding the issue of whether the subthreshold issue is the substantial problem in overcoming the stand-by power issue. In many MOS devices we can face a simultaneous increase in the band-to-band tunneling (BTBT) current around the source and drain junctions because there must be shallow junctions in bulk devices or an extremely thin semiconductor layer in silicon-on-insulator (SOI) devices in order to suppress short-channel effects. Readers will find that MOS devices with steep swing values and low BTBT current values often suffer from the low drivability. We must therefore take account of such tradeoff issues in optimizing the device's performance even when we discuss the low-standby energy concept and device applications. The following chapters review theoretical models of various MOSFETs.

Yasuhisa Omura, Abhijit Mallik, and Naoto Matsuo.

MOS Devices for Low-Voltage and Low-Energy Applications, First Edition.

<sup>© 2017</sup> John Wiley & Sons Singapore Pte. Ltd. Published 2017 by John Wiley & Sons Singapore Pte. Ltd.

### References

- [1] S. M. Sze and K. K. Ng, "Physics of Semiconductor Devices," 3rd ed. (John Wiley & Sons, Inc., 2007), Chapter 6.
- [2] Y. Tsividis, "Operation and Modeling of the MOS Transistor," 2nd ed. (Oxford University Press, 1999).
- [3] J.-P. Colinge, "Silicon-on-Insulator Technology: Materials to VLSI," 3rd ed. (Kluwer Academic Pubishers, 2004).
- [4] T. Sakurai, A. Matsuzawa, T. Douseki (eds.) "Fully-Depleted SOI CMOS Circuits and Technology for Ultralow-Power Applications," (Springer, 2006), pp. 23–58.
- [5] J.-P. Colinge (ed.) "FinFETs and Other Multi-Gate Transistors" (Springer, 2008), Chapters 1 and 2.
- [6] S. Deleonibus (ed.) "Electronic Device Architectures for Nano-CMOS Era from Ultimate CMOS Scaling to beyond CMOS Devices" (Pan Stanford Publishing, 2009).
- [7] A. C. Seabaugh, "Low-voltage tunnel transistors for beyond CMOS logic," *Proc. IEEE*, vol. 98, pp. 2095–2110, 2010.

## 5

### Bulk MOSFET

### 5.1 Theoretical Basis of Bulk MOSFET Operation

Figure 5.1 shows a schematic cross section of a bulk n-channel metal oxide semiconductor field-effect transistor (MOSFET). In the following, we assume an n-channel MOSFET. As there is a single channel inside the body, there are three current flows at the onset of inversion: the front-channel current, the band-to-band tunneling (BTBT) currents at the front interface of the drain junction, and double injection currents at the source junction. In the subthreshold region, the subthreshold current is at the front interface. This chapter focuses on the DC characteristics of bulk MOSFET, and presents a theoretical analysis of the subthreshold and post-threshold current characteristics as an aid to low-energy device design.

### 5.2 Subthreshold Characteristics: "OFF State"

### 5.2.1 Fundamental Theory

Many papers have described the basic features of the subthreshold characteristics of bulk MOSFETs [1, 2]. The input capacitance consists of four components in series: (i) the capacitance of the gate insulator; (ii) the capacitance of the channel depletion layer; (iii) the capacitance of the depletion layer of the source junction (this is available when there exists potential difference between the source terminal and the substrate), and (iv) the capacitance of the depletion layer of the depletion layer of the distribution [2].

In the subthreshold regime, the drain current (Figure 5.2) is given by

$$I_{D(sub)} = I_{D(sub), front} + I_{D(sub), other}$$
(5.1)

Yasuhisa Omura, Abhijit Mallik, and Naoto Matsuo.

MOS Devices for Low-Voltage and Low-Energy Applications, First Edition.

<sup>© 2017</sup> John Wiley & Sons Singapore Pte. Ltd. Published 2017 by John Wiley & Sons Singapore Pte. Ltd.



**Figure 5.1** Bulk MOSFET-cross-section and operation. A: normal front channel, C: avalanche and band-to-band tunnel current (front side), and E: double injection on parasitic bipolar action.



**Figure 5.2** Subthreshold and off-state current characteristics of bulk MOSFET. (With kind permission from Springer Science+Business Media: Fully-Depleted SOI CMOS Circuits and Technology for Ultralow-Power Applications, 2006, pp. 48–58, Yasuhisa Omura (edited by T. Sakurai, A. Matsuzawa, and T. Douseki),© 2006 Springer.)

where  $I_{D(sub),front}$  is the subthreshold current near the front interface and  $I_{D(sub),other}$  is the combined current attributable to parasitic phenomena, such as a simple avalanche at the drain junction [3, 4], BTBT at the drain junction [5, 6] and the generation-recombination (GR) process [7]. For simplicity, this discussion will focus on  $I_{D(sub),front}$ . For an n-channel MOSFET, it is

$$I_{D(sub),front} = -qAD_n \frac{dn}{dy} = qAD_n \frac{n(0) - n(L_{eff})}{L_{eff}}$$
(5.2)

where A is the cross-sectional area of the channel, q is the elementary charge,  $D_n$  is the diffusion constant of electrons,  $L_{eff}$  is the effective channel length, and n(0) and  $n(L_{eff})$  are the electron concentrations at the edges of the source and drain, respectively. They are given by

$$n(0) = n_i \exp\left[\frac{\left(E_F - E_i + q\varphi_{s,front}\left(x = 0, y = 0\right)\right)}{k_B T}\right]$$
(5.3)

and

$$n\left(L_{eff}\right) = n_i \exp\left[\frac{\left(E_F - E_i + q\varphi_{s,front}\left(x = 0, y = 0\right) - qV_D\right)}{k_B T}\right]$$
(5.4)

where  $\varphi_{s,front}$  is the surface potential at the top surface,  $n_i$  is the intrinsic carrier density,  $E_F$  is the Fermi level,  $E_i$  is the intrinsic Fermi level,  $k_B$  is the Boltzmann's constant, and T is the temperature in K. If we assume the effective channel depth to be  $k_B T/qE_s$  [8], where  $E_s$  is the surface electric field [9], the subthreshold current can be written as

$$I_{D(sub),front} = \mu_n \left(\frac{W_{eff}}{L_{eff}}\right) q \left(\frac{k_B T}{q}\right)^2 \left(\frac{n_i^2}{N_A}\right) \left\{1 - \exp\left[\frac{-qV_D}{k_B T}\right]\right\} \frac{\exp\left[\frac{q\varphi_{s,front}}{k_B T}\right]}{E_s}$$
(5.5)

where  $\mu_n$  is the electron mobility calculated from the Einstein relation  $D_n = \mu_n k_B T/q$ ,  $N_A$  is the doping concentration of substrate,  $W_{eff}$  is the channel width, and  $V_D$  is the drain voltage. We can derive the following basic expression for the subthreshold swing (SS) from Eq. (5.5) if we neglect the influence of interface states for simplicity.

$$SS = \left(\frac{kT}{q}\right) \ln\left(10\right) \left\{1 + \frac{C_s}{C_{ox}}\right\}$$
(5.6)

where

$$C_s = \frac{\varepsilon_s}{W_D} \tag{5.7}$$

 $C_{ox}$  (= $\varepsilon_{ox}/t_{ox}$ ) is the capacitance of the gate oxide layer,  $C_s$  is the depletion capacitance of the substrate,  $t_{ox}$  is the thickness of the gate oxide layer,  $\varepsilon_s$  is the permittivity of semiconductor, and  $W_D$  is the depletion layer width. As seen in Eq. (5.6), the basic expression for SS depends on doping concentration of the substrate, gate oxide layer thickness, permittivity of the gate oxide layer, and permittivity of the substrate.

The main conclusions that can be drawn from Eq. (5.6) are:

• Influence of gate oxide thickness  $(t_{ox})$  on SS. One of the most common ways to suppress short-channel effects is to reduce  $t_{ox}$ , which makes  $C_s/C_{ox}$  small, as shown by Eq. (5.6). This means that the  $t_{ox}$  leads to the straightforward reduction of SS.



Figure 5.3 Dynamic-threshold MOSFET. (a) Cross section and (b) characteristics.

- Influence of doping concentration  $(N_A)$  on SS. Another common way to suppress shortchannel effects is to increase  $N_A$ . This often causes SS to increase. To prevent that,  $t_{ox}$  should also be reduced when  $N_A$  is increased.
- Influence of substrate potential on *SS*: dynamic-threshold (DT) MOSFET operation (Figure 5.3). The substrate potential is often set to a certain value. In that case, *SS* is almost independent of the front gate voltage, but depends on the device parameters. In a dynamic-threshold MOSFET [10], the substrate terminal is connected to the front gate electrode; so, the substrate potential increases with the front gate voltage. This increase reduces the built-in potential of the source junction, thereby increasing the channel current. So, a simplified expression for the subthreshold current of a dynamic threshold MOSFET is

$$I_{D(sub),DT} = I_{D(sub),front} C_0 \exp\left[\frac{qV_{FG}}{mk_BT}\right]$$
(5.8)

where

$$I_{D(sub),front} = \mu_n \left(\frac{W_{eff}}{L_{eff}}\right) q \left(\frac{k_B T}{q}\right)^2 \left(\frac{n_i^2}{N_A}\right) \left\{1 - \exp\left[\frac{-qV_D}{k_B T}\right]\right\} \frac{\exp\left[\frac{q\varphi_{s,front}\left(x=0, y=0, V_{FG}\right)}{k_B T}\right]}{E_s}$$
(5.9)

 $C_0$  is a constant, *m* is the ideality factor (*m*>1), and  $\varphi_s(x=0, y=0, V_{FG})$  is the surface potential modified by  $V_{FG}$ . It should be noted that the subthreshold channel region depends on the initial surface condition of the device because the front gate voltage does not change the band structure near the top surface drastically. This is an important aspect of the dynamic threshold MOSFET. An approximate expression for the *SS* of a dynamic threshold MOSFET is

$$SS = \eta \left(\frac{k_B T}{q}\right) \ln(10) \left[1 + \frac{C_s}{C_{ox}}\right]$$
(5.10)

where  $\eta < 1$  and  $C_s$  is given by Eq. (5.7).

• Drain-induced barrier lowering (DIBL) (front interface) (Figure 5.4). In a short-channel bulk MOSFET, DIBL [11] near the source junction at the front interface significantly degrades the SS. The reason for this is that the drain-induced lateral electric field extends quite far into the channel region. There are two ways to suppress the DIBL: one is to make  $N_A$  higher, and the other is to replace the gate oxide with a high- $\kappa$  material. However, the former degrades the SS because  $C_s$  increases in Eq. (5.6). Therefore, the pocket ion-implantation technique [12] is frequently introduced in order to suppress the extension of the drain-induced lateral electric field.

### 5.2.2 Influence of BTBT Current

Band-to-band tunneling often occurs in the gate-drain overlap region [13]. It is sometimes called the gate-induced drain leakage (GIDL) current. For MOSFETs with a thin gate oxide, it has a significant influence on DC and AC operation [14]. An empirical expression for this current is [15]

$$I_{D(sub),others} = A_0 E_{SS} \exp\left[\frac{-B_0}{E_{SS}}\right]$$
(5.11)

where  $A_0$  and  $B_0$  are constants that depend on the device parameters and  $E_{ss}$  is the surface electric field of the gate overlap region. As the gate oxide of recent MOSFETs tends to be very thin, the electric fields of the gate-drain and drain-source overlap regions are higher than those of past devices. As a result, the contribution of the BTBT current to the subthreshold characteristics is apt to be significant [16].



**Figure 5.4** Drain-induced barrier lowering phenomenon in the bulk MOSFET. (a) Schematic view of DIBL and (b) impact of DIBL on the surface potential profile.

### 5.2.3 Points to Be Remarked

The "OFF state" current in the subthreshold region limits the standby power of the MOSFET even when the threshold voltage is sufficiently high. In the case of the bulk MOSFET, the reverse-biased leakage current generated at a large metallurgical junction area, the weak avalanche-based current, and the BTBT current around the gate-overlapped region of the drain diffusion region shares a large part of the total leakage current. These are apt to increase when the short-channel effects are suppressed because the suppression of the short-channel effects raises the local electric field around the drain diffusion. Therefore the lowering of the drain voltage is requested for the purpose of the suppression of those leakage current components. These points will be discussed again later.

### 5.3 Post-Threshold Characteristics: "ON State"

### 5.3.1 Fundamental Theory

In the post-threshold regime, the drain current is given by

$$I_{D(post)} = I_{D(post), front} + I_{D(post), other}$$
(5.12)

where  $I_{D(post),front}$  is the inversion channel current along the front interface and  $I_{D(post),other}$  is the parasitic current, which consists of the leakage current of the reverse-biased drain junction [17], a parasitic bipolar current [18], and an avalanche current [19]. The discussion below focuses on  $I_{D(post),front}$ .

In practice, the post-threshold channel current consists mainly of the drift current, where carriers are accelerated by the drain-to-source electric field. It is analyzed in the conventional gradual channel approximation. The expression for the drain current of the bulk MOSFET is derived below.

We start from the Ohmic relation

$$I_{D(post),front} = -W_{eff} \mu_n Q_n \left(V\right) \frac{dV(y)}{dy}$$
(5.13)

where V(y) is the local channel potential and  $Q_n(V)$  is the local electronic charge density. This is the expression for the local current inside the device, if we neglect the diffusion and other currents like the generation-recombination current.

We obtain the following relation for  $Q_{u}(V)$  from Poisson's equation for the channel region [20]:

 $Q_n$  = total induced charge density of semiconductor – depletion charge density of substrate,

$$= -C_{ox}\left(V_{FG} - V_{FB,front} - \varphi(0) - V\right) + qN_A W_D\left(\varphi(0) + V\right)$$
(5.14)

Integrating it from source to drain based on the current continuity, we obtain the following expression for  $I_{D(post),front}$ :

$$I_{D(post),front} = \left(\frac{W_{eff}}{L_{eff}}\right) \mu_n C_{ox} \left[V_{FG} - V_{TH}^* - \frac{V_D}{2}\right] V_D + \left(optional - term\right)$$
(5.15)

where

$$V_{TH}^{*} = V_{FB,front} + \varphi_{s,front} \left(x = 0, y = 0\right) + \frac{\sqrt{2q\varepsilon_{s}N_{A}\varphi_{s,front} \left(x = 0, y = 0\right)}}{C_{ox}} + \left(optional - term\right)$$
(5.16)

When the doping level near the surface is not so high, substituting the new expression for  $Q_n(V)$  into the Ohmic relation (5.13), and assuming current continuity, yield the following expression for  $I_{D(post)}$  front:

$$I_{D(post),front} = \left(\frac{W_{eff}}{L_{eff}}\right) \mu_n C_{ox} \left[V_{FG} - V_{TH,front} - \frac{V_D}{2}\right] V_D$$
(5.17)

where the threshold voltage of a MOSFET  $(V_{TH,front})$  is

$$V_{TH,front} = V_{FB,front} + \varphi_{s,front} \left( x = 0, y = 0 \right) + \frac{q N_A W_D \left[ \varphi_{s,front} \left( x = 0, y = 0 \right) \right]}{C_{ox}}$$
(5.18)

The saturated drain current  $(I_{D(post)sat})$  is given by:

$$I_{D(post)sat} = \left(\frac{W_{eff}}{2(1+\alpha)L_{eff}}\right) \mu_n C_{ox} \left[V_{FG} - V_{TH,front}\right]^2$$
(5.19)

where  $\alpha$  is the factor depending on the substrate doping concentration profile. When the substrate has a uniform doping profile and its doping concentration is not so high,  $\alpha \rightarrow 0$ . The drain current of the bulk MOSFET on the saturation condition is basically independent of the drain voltage  $(V_D)$  as far as short-channel effects are not seen. Other important factors are discussed below.

### 5.3.2 Self-Heating Effects

Powered devices suffer from self-heating effects as shown in Figure 5.5. In the bulk MOSFET, the thermal conductivity of the substrate is not so high [21]. According to simulations [22], the temperature near the drain junction quickly rises to 100 °C. Since self-heating effects degrade the surface mobility of carriers, they must be taken into account. In electrostatic-discharge (ESD) protection circuits, self-heating effects reduce the temperature margin for the second breakdown. So, adequate thermal paths must be added during metallization.

If we need to take into account the influence of self-heating effects on drain current, we have to use the following expression for the mobility [23]:

$$\mu_{n(self-heating)} = C_1 \left[ T_0 + \theta I_{D(post), front} V_D \right]^{-\delta}$$
(5.20)

where  $C_1$  is a constant,  $T_0$  is room temperature, and  $\theta$  and  $\delta$  are fitting parameters.



**Figure 5.5**  $I_p$ - $V_p$  characteristics of bulk MOSFET.



**Figure 5.6** Parasitic bipolar action in the n-channel bulk MOSFET. Avalanche-induced holes (C) are injected into the source (E), and electrons are injected into the body (A). This positive feedback loop turns on parasitic bipolar action.

### 5.3.3 Parasitic Bipolar Effects

When the drain-to-source voltage is high, the electric field around the drain pn junction takes a high value. In the depletion region around the drain pn junction, a weak avalanche multiplication of carriers takes place. In that case, as shown in Figure 5.6, most holes generated near the drain are absorbed to the bulk substrate ("C" in Figure 5.6) and they are collected at the substrate terminal; this is the so-called "substrate current." However, some holes flow into the source junction ("E" in Figure 5.6). When the substrate resistivity is high, the body potential automatically rises by the substrate current. When the "forward-biased" current is made at the source junction, it works as the "base current" of the "NPN" parasitic bipolar transistor. This frequently results in a fatal "burnout" phenomenon.

### 5.4 Comprehensive Summary of Short-Channel Effects

Considering a simple phenomenalistic model of short-channel effects, we obtain

$$V_{TH} = V_{FB,front} + f_{DIBL}\varphi_{s,front} \left(x = 0, y = 0\right) + f_{CS} \frac{qN_A W_D \left[\varphi_{s,front} \left(x = 0, y = 0\right)\right]}{C_{ox}} - \eta V_{BG}^{'}$$
(5.21)

where  $f_{DIBL}$  is the DIBL factor,  $f_{CS}$  is the charge-sharing factor, and  $\eta$  is the factor expressing the impact of the substrate bias effect.

### References

- [1] S. M. Sze and K. K. Ng, "Physics of Semiconductor Devices," 3rd ed. (John Wiley & Son, Inc., 2007), Chapter 6.
- [2] Y. Tsividis, "Operation and Modeling of the MOS Transistor," 2nd ed. (Oxford University Press, 1999).
- [3] S. M. Sze and G. Gibbons, "Avalanche breakdown voltages of abrupt and linearly graded p-n junctions in Ge, Si, GaAs, and GaP," *Appl. Phys. Lett.*, vol. 8, pp. 111–113, 1966.
- [4] G. Merckel, F. Van de Wiele, W. Engl, and P. Jespers, "NATO Course on Process and Device Modeling for Integrated Circuit Design," (Noordhoff, 1975), p. 725.
- [5] L. Esaki, "New phenomenon in narrow germanium p-n junctions," Phys. Rev., vol. 109, p. 603, 1958.
- [6] E. O. Kane, "Theory of tunneling," J. Appl. Phys., vol. 32, pp. 83-91, 1961.
- [7] W. Shockley and W. T. Read, Jr., "Statistics of the recombination of holes and electrons," *Phys. Rev.*, vol. 87, pp. 835–842, 1952.
- [8] S. M. Sze and K. K. Ng, "Physics of Semiconductor Devices," 3rd ed. (John Wiley & Sons, Inc., 2007), p. 314.
- [9] S. M. Sze and K. K. Ng, "Physics of Semiconductor Devices," 3rd ed. (John Wiley & Sons, Inc., 2007), p. 301.
- [10] F Assaderaghi, D. Sinitsky, S. A. Parke, J. Boker, P. K. Ko, and C. Hu, "A Dynamic Threshold Voltage MOSFET (DTMOS) for Ultra-Low Voltage Operation," Tech. Dig. Int. Electron Devices Meeting (San Francisco, Dec., 1994) pp. 809–812, 1994.
- [11] G. W. Taylor, "Subthreshold conduction in MOSFET's," *IEEE Trans. Electron Devices*, vol. 25, pp. 337–350, 1978.
- [12] T. Hori, "A 0.1 µm CMOS Technology with Tilt-Implanted Punchthrough Stopper (TIPS)," Tech. Dig., IEEE IEDM (San Francisco, 1994) pp. 75–78, 1994.
- [13] E. Takeda, H. Matsuoka, and S. Asai, "A Band to Band Tunneling MOS Device (B<sup>2</sup>T-MOSFET)-A Kind of 'Si quantum Device'," Tech. Dig., IEEE IEDM (San Francisco, 1988) pp. 402–405, 1988.
- [14] M. Chan, J. Lin, S. N. Shih, T.-C. Wu, B. Huang, J. Yang, and P.-I. Lee, "Impact of gate-induced drain leakage on retention time distribution of 256 Mbit DRAM with negative wordline bias," *IEEE Trans. Electron Devices*, vol. 50, pp. 1036–1041, 2003.
- [15] H.-J. Wann, P.-K. Ko, and C. Hu, "Gate-Induced Band-to-Band Tunneling Leakage Current in LDD MOSFETs," Tech. Dig. IEEE IEDM (San Francisco, 1992) pp. 147–150, 1992.
- [16] J. Chen, F. Assaderaghi, P.-K. Ko, and C. Hu, "The enhancement of Gate-Induced-Drain-Leakage (GIDL) current in short-channel MOSFET and its application in measuring lateral bipolar current gain," *IEEE Electron Device Lett.*, vol. 11, pp. 572–574, 1992.
- [17] S. M. Sze and K. K. Ng, "Physics of Semiconductor Devices," 3rd ed. (John Wiley & Sons, Inc., 2007), pp. 90-114.
- [18] L. Wakeman, "Silicon-gate CMOS chips gain immunity to SCR latchup," *Electronics*, vol. 56, pp. 136–140, 1983.
- [19] S. M. Sze and K. K. Ng, "Physics of Semiconductor Devices," 3rd ed. (John Wiley & Sons, Inc., 2007), pp. 104–106.
- [20] S. M. Sze and K. K. Ng, "Physics of Semiconductor Devices," 3rd ed. (John Wiley & Sons, Inc., 2007), pp. 298–303.
- [21] D. Sharma, J. Gautier, and C. Merckel, "Negative resistance in MOS devices," *IEEE J. Solid-State Circuits*, vol. SC-13, pp. 378–380, 1978.
- [22] D. Sharma and K. Ramanathan, "Modeling thermal effects on MOS I-V characteristics," *IEEE Electron Device Lett.*, vol. EDL-4, p. 362, 1983.
- [23] R. van Langevelde and F. M. Klaassen, "Accurate Drain Conductance Modeling for Distortion Analysis in MOSFETs," Tech. Dig. IEEE IEDM (Washington, D. C., 1997) pp. 313–316, 1997.

## 6

## SOI MOSFET

### 6.1 Partially Depleted Silicon-on-Insulator Metal Oxide Semiconductor Field-Effect Transistors

The partially depleted (PD) n-channel silicon-on-insulator metal oxide semiconductor fieldeffect transistor (SOI MOSFET) has a quasineutral region in the silicon-on-insulator (SOI) layer as shown in Figure 6.1. This configuration is very similar to that of the bulk metal oxide semiconductor field-effect transistor (MOSFET) except for the buried oxide layer beneath the device region. Therefore, most operation characteristics are similar to those of the bulk MOSFET. However, the device has a few different characteristics from the bulk MOSFET, such as the kink in  $I_D$  versus  $V_D$  characteristics [1–4] and the body-floating characteristics [1–4]; that is, the potential of the quasineutral region is not fixed to a specific potential. When the potential of the quasineutral region floats, the potential of the quasineutral region of the SOI MOSFET cannot respond quickly to changes in the gate electrode and the drain electrode, which slows the operation of the partially depleted SOI MOSFET [5].

When a positive bias is applied to the substrate, the depletion layer expands from the bottom surface of the silicon layer, which yields an optional leakage current path on the bottom surface of the silicon layer. We have to increase the body doping concentration near the bottom surface of the silicon layer in order to suppress this optional leakage current [6]. When a high positive bias is applied to the substrate, the silicon body can be fully depleted [6]. When the full depletion of the silicon body is held, the SOI MOSFET exhibits the specific characteristics described in the following section.

MOS Devices for Low-Voltage and Low-Energy Applications, First Edition.

Yasuhisa Omura, Abhijit Mallik, and Naoto Matsuo.

© 2017 John Wiley & Sons Singapore Pte. Ltd. Published 2017 by John Wiley & Sons Singapore Pte. Ltd.