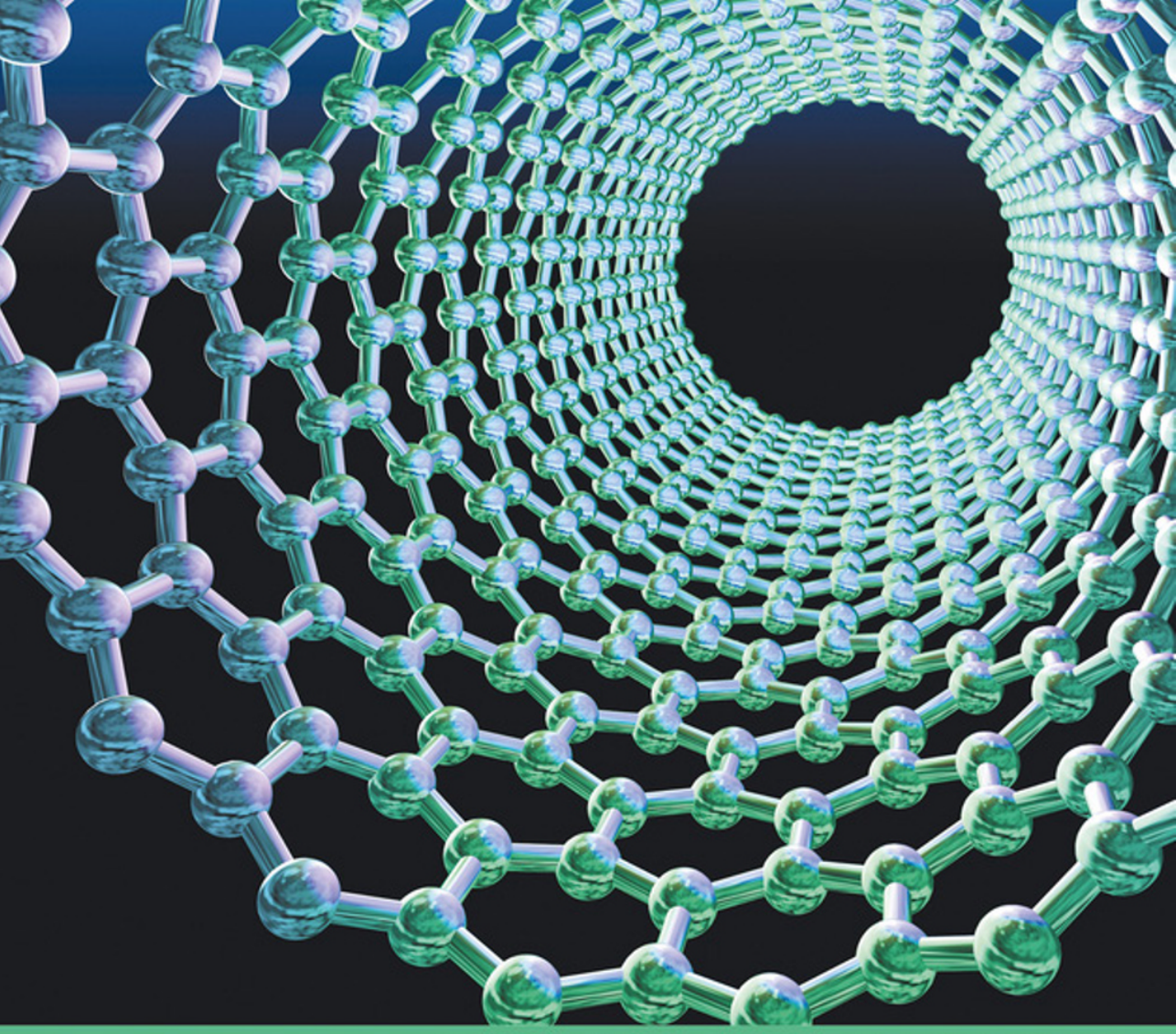

HIDEAKI TSUCHIYA | YOSHINARI KAMAKURA

Carrier Transport in Nanoscale MOS Transistors

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Hideaki Tsuchiya

Yoshinari Kamakura

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Preface

The device scaling concept, which can lead to increase in both switching speed and integrated density of MOSFETs with reasonable power consumption, has been the main guiding principle of the integrated device engineering over the past 40 years. It has been recognized, however, that conventional device scaling has confronted difficulties below the sub-100 nm regime, owing to several physical and essential limitations directly related to device miniaturization. As a consequence, new device technologies to overcome these difficulties are highly required. A group of these new device technologies, called technology boosters, include high-k gate stack technologies, high carrier mobility channels, ultrathin-body structures, multigate structures, metal source/drain, and novel operating principles. The basic purpose of these technologies are to boost or improve specific device parameters, such as carrier velocity, gate leakage current, short-channel effects, subthreshold slope, and so on.

Given the large number of technology options mentioned above, physically based device simulations will play an important role in developing the most promising strategies for forthcoming nanometer era. In particular, most of the device architecture and material options are expected to affect the performance of MOSFETs through the band structure, the electrostatics and the scattering rates of carriers in the channel region. Therefore, microscopic or atomistic modeling is necessary to obtain a physical insight and to develop a quantitative description of the carrier transport in ultrascaled MOSFETs. In this context, this book aims to offer a thorough explanation of carrier transport modeling of nanoscale MOSFETs, covering topics from the atomistic band structure calculation to the most recent challenges targeting beyond the end of the International Technology Roadmap for Semiconductors (ITRS). We also focus on the roles of phonon transport in ultrascaled MOSFETs, which are getting a lot more attention lately as major thermal management challenges on the LSI chip.

As for the modeling methodology, we have highlighted the multi-subband Monte Carlo method because of some distinct advantages compared to other methods. Specifically, it provides us with the ability to explore all transport regimes, including diffusive, quasi-ballistic and even quantum transport (by applying a Wigner Monte Carlo technique) regimes, and also introduces new scattering mechanisms without increasing its computational resources. The physical interpretation of calculated results is intuitively comprehensible, owing to its particle description of the carrier transport. The dynamical equation of the Wigner function

(i.e. the Wigner transport equation) is very similar to the Boltzmann transport equation, except in the influence of the potential whose rapid space variations generate quantum mechanical effects. Furthermore, it coincides with the non-equilibrium Green's function formalism under a ballistic transport. We have illustrated the details of the Wigner Monte Carlo technique and its application to the quantum transport analysis of III-V MOSFETs in this book.

To go beyond the end of the ITRS roadmap, several alternative or innovative devices are being investigated, such as nanowires, carbon nanotubes, graphenes and tunnel-FETs. We have dealt with nanowires and some atomic layer 2-D materials related to graphene, and have discussed their performance potentials by comparisons with those of competitive MOSFETs composed of Si and III-V compound semiconductors.

This book was written for graduate students, engineers and scientists who are engaged in work on nanoscale electronic devices, and was designed to provide a deeper understanding of physical aspects of carrier transport in real electronic devices. Familiarity with quantum mechanics, basic semiconductor physics and electronics is assumed. After working through this book, students should be prepared to follow current device research, and to actively participate in developing future devices.

Hideaki Tsuchiya
Yoshinari Kamakura

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1

Emerging Technologies

1.1 Moore's Law and the Power Crisis

Figure 1.1 shows the famous Moore's law for a metal-oxide-semiconductor field-effect transistor (MOSFET) integrated in an electronic logic circuit, which illustrates the annual variations in the number of transistors and in transistor size in a simple way. Since large-scale integrated (LSI) circuit technology was invented in the 1960s, the progress of miniaturization techniques based on scaling law has achieved significant advancement in the electronics industry, up to the present date. However, from the year around 2005, the increase in power consumption of LSI circuits has become a major problem. To succeed in the scaling law, not only the geometrical dimensions of MOSFET, a basic building block of LSI circuit, but also their power supply voltage, are required to be scaled down simultaneously. However, the power supply voltage has ceased to fall, at around 1 V after 2005. There are various reasons for this – for example: to suppress characteristic variability among hundreds of millions of integrated MOSFETs; to cut wasteful power consumption in the off-state; to maintain high-speed performance, and so on. Consequently, LSI consumption power or, in terms of global influence, the total electrical power consumed by IT devices and systems all over the world, increases rapidly year by year.

The power consumption of a MOSFET is expressed by:

$$P = f C_{\mathrm{load}} V_{\mathrm{dd}}^2 + I_{\mathrm{off}} V_{\mathrm{dd}} \tag{1.1}$$

where f, C_{load}, V_{dd} and I_{off} represent the operating frequency, the load capacitance, the power-supply voltage, and the off-current, respectively. The first term on the right-hand side of Equation (1.1) corresponds to the power required to charge and discharge a MOS capacitor, (i.e., a consumed power at on-state), and the second term, consumed power at off-state. The ceasing to fall of V_{dd}, as mentioned above, has mainly induced the increase in consumed power at on-state. On the other hand, owing to the drain-induced barrier lowering (DIBL)

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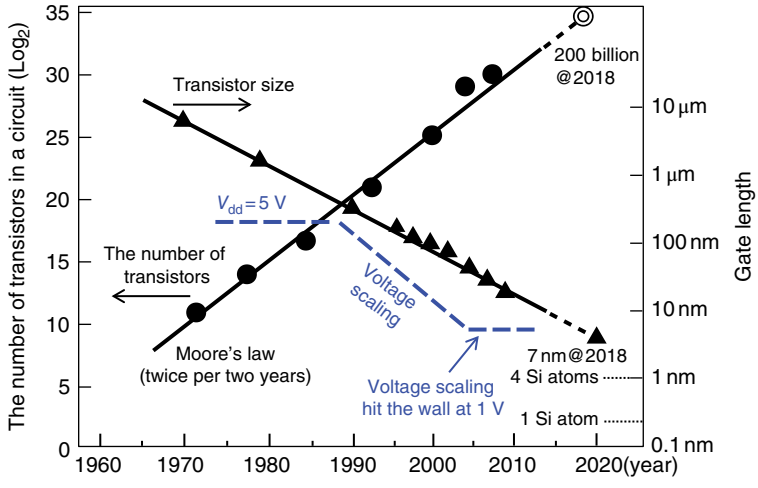

Figure 1.1 Moore's law for a MOSFET integrated in a LSI.

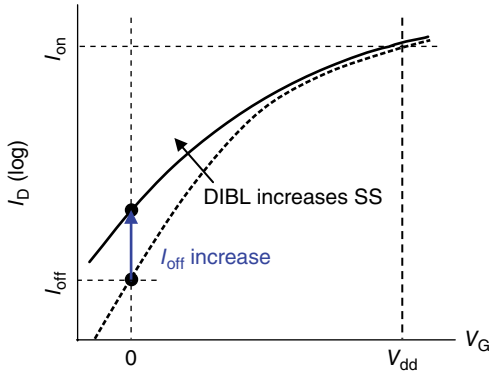

Figure 1.2 Influences of DIBL on $I_D - V_G$ characteristics. DIBL degrades the subthreshold slope (SS) and then causes an exponential I_{off} increase.

phenomenon, which is caused by reduction of the gate electrostatic control over the channel with decreasing the channel length, I_{off} is beginning to increase exponentially, as shown in Figure 1.2. This leads to a drastic increase in consumed power at off-state – which, for instance, decreases the battery life of mobile devices such as smartphones and wearable appliances.

1.2 Novel Device Architectures

To reduce the off-state power consumption, novel structure MOSFETs that possess better gate electrostatic control to suppress DIBL have received a lot of attention [1.1]. The representative new device structures are shown in Figure 1.3. In 2012, the Intel Corporation released an announcement stating that they were starting to manufacture central processing units (CPUs)

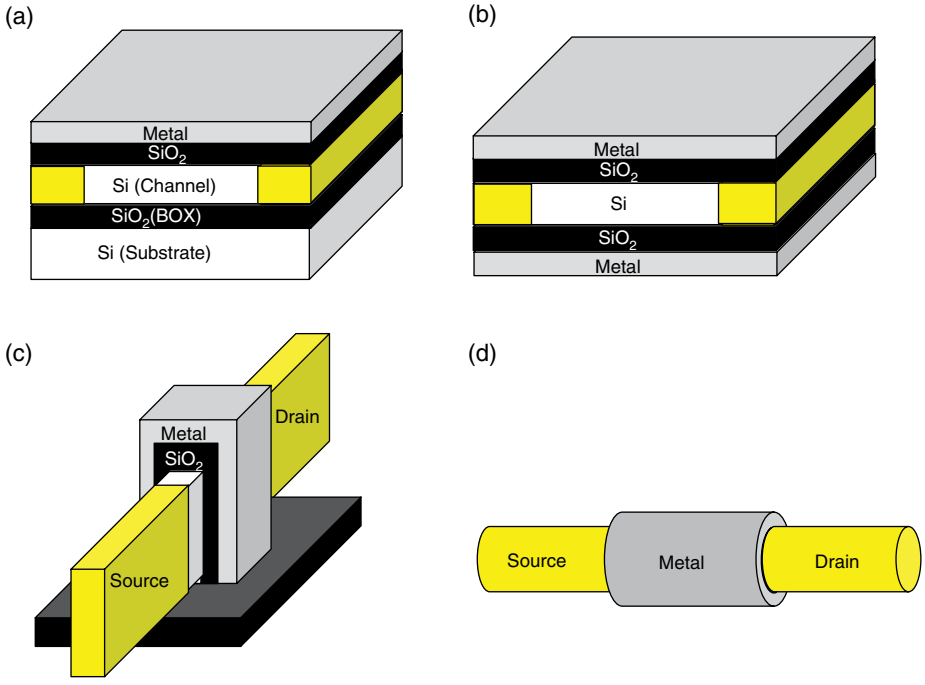

Figure 1.3 Representative new device structures. (a) ultrathin-body (UTB) silicon-on-insulator (SOI) structure; (b) double-gate (DG) structure; (c) Fin or trigate structure; and (d) gate-all-around (GAA) nanowire structure.

constructed from FinFETs [1.2]. This was a landmark in the electronic industry, because a three-dimensional transistor has been commercialized for the first time since the planar type MOS transistor was invented in 1960. A GAA nanowire MOSFET, shown in Figure 1.3(d), is considered one of the ultimate structures of FinFETs and, therefore, globally active and competitive research has been promoted.

As seen in Figure 1.3, these new structure MOSFETs have an ultrathin Si channel sandwiched in between gate oxides or insulators of substrate. In particular, Si channels in FinFET and GAA nanowire MOSFET are completely surrounded by oxides. As a result, the Si channel thickness T_{Si} fluctuates along a transport direction in atomic scale, as shown in Figure 1.4.

When T_{Si} is thinner than a spatial extent of carrier's wave function, the T_{Si} fluctuation produces spatial fluctuation of quantized sub-band along the transport direction, and thus leads to an additional scattering source for carriers. Consequently, the carrier mobility may seriously decrease in nanometer-scaled new structure MOSFETs. The influence of the T_{Si} fluctuation was first investigated by H. Sakaki *et al*. experimentally and theoretically for GaAs/AlAs quantum well structures [1.3]. They found that the electron mobility reduces in proportion to the sixth power of quantum well thickness, which shows that the interface fluctuation scattering is the dominant scattering mechanism in thin quantum well structures.

For SOI-MOSFETs, K. Uchida *et al*. experimentally demonstrated that the same channel thickness dependence as for Sakaki's result is obtained for T_{Si}s less than 3 nm, as shown in

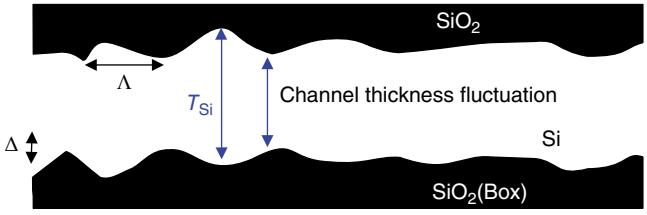

Figure 1.4 Spatial fluctuation of Si channel thickness along transport direction, which emerges in ultrathin Si films with a nanometer thickness.

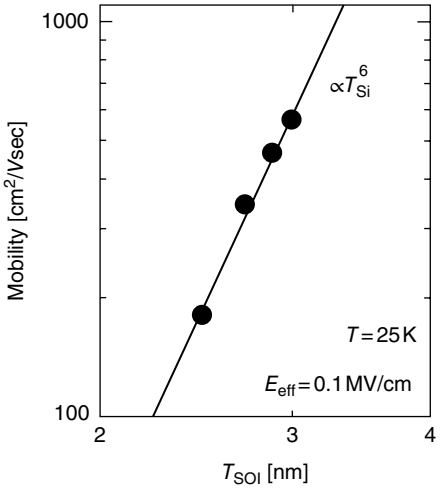

Figure 1.5 T_{Si} dependence of electron mobility at 25 K [1.4]. $T_{Si}{}^{6}$ dependence is clearly observed for T_{Si}s less than 3 nm.

Figure 1.5 [1.4]. Therefore, there are growing concerns about the degradation of the on-state device performance in new structure MOSFETs with a nanometer channel thickness. However, the role of the T_{Si} fluctuation under a quasi-ballistic transport, where scattering events inside the channel decrease to several times, has not yet been fully understood. To deeply understand it, we need to develop a device simulation technique considering quantum confinement and scattering effects at the atomic level. We will describe such a challenge in Chapter 3.

In addition to the scattering by the T_{Si} fluctuation mentioned above, phonon scattering and impurity scattering also play an important role. In particular, intrinsic channels are likely adopted in novel structure MOSFETs and, thus, deep understanding of phonon scattering processes in ultrashort channel MOSFETs should be important. Carrier transport in this regime has been actively discussed in terms of the quasi-ballistic transport since K. Natori proposed the concept of ballistic MOSFET [1.5].

As for phonon scattering processes, interestingly, *inelastic phonon emission processes* can suppress carriers backscattering to the source and then promote ballistic transport, contrary to common sense, in the case of ultrashort-channel MOSFETs [1.6, 1.7]. This is considered to be

due to the fact that once a carrier has lost its kinetic energy by a few multiples of k_BT (about 60 meV for silicon) via inelastic phonon emission processes, the carrier has little chance of returning to the source, due to the potential bottleneck barrier, and is eventually absorbed into the drain; thus, the ballisticity improves. We will discuss this subject in detail in the first half of Chapter 3.

The continued scaling of transistor dimensions and integrated density is causing major thermal management challenges on the LSI chip [1.8]. In particular, the novel structure MOSFETs have Si channels surrounded by the gate oxides and insulators, which have a lower thermal conductivity than Si [1.9]. Therefore, thermal energies generated in a device via optical phonon emission are readily accumulated inside the device, which might lead to degradation of the device performance. In Chapter 4, we will discuss phonon transport in Si nanostructures, to examine such a heat generation problem qualitatively.

1.3 High Mobility Channel Materials

The reduction of V_{dd} is essential to decrease on-state power consumption. Higher mobility channel materials can increase the on-current because the carrier's velocity becomes higher at the same V_{dd}, and thus they are expected to achieve equal or superior performance to Si MOSFETs under a lower V_{dd} operation [1.10], as shown in Figure 1.6.

The effective masses and mobilities of representative semiconductors are summarized in Table 1.1. Compared to Si, Ge has both a higher electron mobility and a higher hole mobility, while III-V compound semiconductors, that is, InP and $In_{0.53}Ga_{0.47}As$, have a significantly higher electron mobility. One of the important reminders is that the solid solubility of donors in III-V semiconductors is limited to less than, or comparable to, $2\times10^{19}\,cm^{-3}$ [1.11]. Consequently, III-V MOSFETs generally exhibit a higher parasitic resistance in source and drain electrodes than Si MOSFETs do [1.12–1.15]. This also may lead to "source starvation" [1.12, 1.13], which cannot maintain a large flow of ballistic carriers heading in the channel, owing to the insufficient impurity scattering in the lightly doped source. We will discuss this subject in the first half of Chapter 5.

The higher mobilities of III-V semiconductors are mainly due to their lighter effective masses. But then, a lighter effective mass carrier has a larger tunneling probability through a

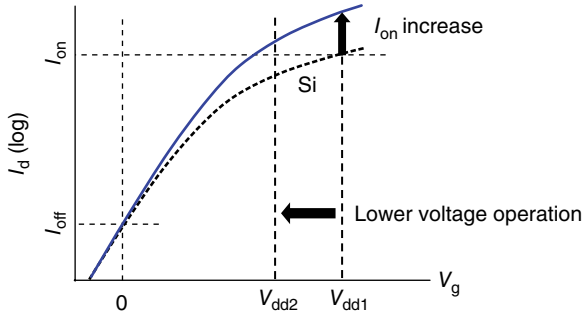

Figure 1.6 On-current increase due to high-mobility channel MOSFETs. They are expected to achieve a lower V_{dd} operation than conventional Si MOSFETs.

Table 1.1 Effective masses and mobilities of representative semiconductors.

Material		Si	Ge	InP	$In_{0.53}Ga_{0.47}As$
electron	mass m_e (m_0)	0.19/0.98 (m_t/m_l)	0.082/1.59 (m_t/m_l)	0.082	0.046
	mobility ($cm^2/V \cdot s$)	1600	3900	5400	25 000
hole	mass m_{hh}/m_{lh} (m_0)	0.49/0.16	0.28/0.044	0.45/0.12	0.51/0.22
	mobility ($cm^2/V \cdot s$)	430	1900	200	450

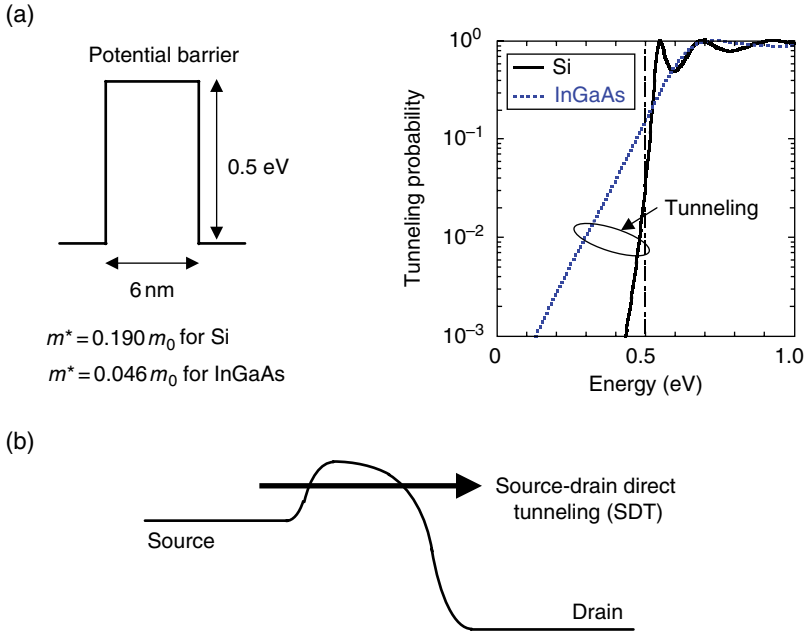

Figure 1.7 (a) Tunneling probabilities calculated for Si and $In_{0.53}Ga_{0.47}As$ through a single potential barrier and (b) schematic of source-drain direct tunneling (SDT) at off-state.

finite potential barrier. Figure 1.7(a) shows the tunneling probabilities calculated for Si and $In_{0.53}Ga_{0.47}As$ through the potential barrier with 0.5 eV height and 6 nm width, which supposes an off-state of a sub-10 nm MOSFET. The effective masses were given as $m^* = 0.19\, m_0$ for Si and $0.046\, m_0$ for $In_{0.53}Ga_{0.47}As$.

It is found that $In_{0.53}Ga_{0.47}As$ exhibits several orders of magnitude larger tunneling probability than Si. This phenomenon leads to a tunneling leakage current between source and drain electrodes at off-state, as shown in Figure 1.7(b). Therefore, this is called "source-drain direct tunneling (SDT)." SDT might be a major obstacle in downscaling III-V MOSFETs into the deca-nanometer or nanometer scale [1.16, 1.17]. We will discuss this subject in the second half of Chapter 5.

1.4 Two-Dimensional (2-D) Materials

Graphene, a one-atom-thick carbon sheet arranged in a honeycomb lattice [1.18], is known to exhibit the highest electron mobility of all presently-known materials and, therefore, its application to high-speed electronic devices is strongly anticipated. However, since graphene has no band gap, the electrical conduction cannot be fully switched off by tuning the gate voltage, which is necessary for digital applications. To open a band gap, several methods have been proposed, as shown in Figure 1.8. Graphene nanoribbon (Figure 1.8(a)) uses quantum confinement effect in its transverse direction, while bilayer graphene (Figure 1.8(b)) introduces symmetry breaking between two carbon layers via a vertical electric field or interaction between a graphene layer and its substrate.

Although these methods actually open a band gap in graphene, the characteristic linear dispersion relation is distorted and, furthermore, an effective mass appears in graphene nanoribbons. Accordingly, accurate consideration of the band structure is important in order to assess the device characteristics of semiconducting graphene devices.

Practical application of graphene devices require a reliable substrate, but the mobility in graphene on SiO_2 substrates is limited to 25 000 cm^2/Vs [1.19–1.21]. The reason for this mobility reduction on SiO_2 substrates is considered to be the additional scattering mechanisms induced by the substrate, such as charged impurities, polar and non-polar surface optical phonons in the SiO_2, and substrate surface roughness. On the other hand, a drastic improvement of the mobility to 140 000 cm^2/Vs near the charge neutrality point was reported using a hexagonal boron nitride (h-BN) substrate [1.22]. Hence, h-BN substrate is expected to be suitable for graphene electronic devices. For practical design and analysis of graphene devices, we will need to consider the scattering from the substrates precisely.

The discovery of graphene, and the succeeding tremendous advancement in this field of research, have promoted the search for similar two-dimensional (2-D) materials composed of other group IV elements. The silicon or germanium equivalents of graphene are called silicene and germanene. A 2-D silicene has been successfully fabricated on (0001)-oriented thin films of zirconium diboride (ZrB_2), that were grown epitaxially on Si (111) wafers [1.23]. Theoretical simulations showed that silicene and germanene have no band gap, similar to graphene. On the other hand, 2-D materials such as silicane, germanane [1.24], MoS_2 [1.25, 1.26] and black phosphorus [1.27, 1.28] exhibit a band gap larger than about 1 eV, though they are monolayer-thick materials. These 2-D materials with a sufficiently large band gap may have advantages in the application to LSI devices over graphene-based materials. We will discuss the electronic properties of 2-D materials and their performance potentials as an FET channel in Chapter 7.

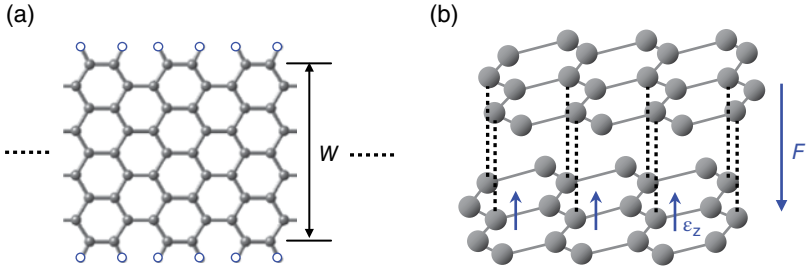

Figure 1.8 (a) Graphene nanoribbon; and (b) bilayer graphene to open a band gap.

1.5 Atomistic Modeling

As described in Section 1.2, Si UTB-SOI MOSFET, shown in Figure 1.3 (a) has better gate electrostatic control over the channel than conventional Si bulk MOSFET, and thus is expected to be immune to short-channel effects such as DIBL, and threshold voltage lowering with decreasing the channel length. Experimentally, extremely-scaled SOI-MOSFETs with Si channel thickness less than 1 nm have been fabricated, as shown in Figure 1.9(a) [1.29].

Currently, hydrogen termination of the channel is used in device modeling, as a compromise between efficiency and accuracy. However, in such atomic-scale dimensions, not only the quantum confinement effects, but also the roles of interfaces between the Si channel and the SiO_2 oxides, will be important to achieve good agreement with experimental results. Thus, state-of-the-art *ab initio* simulation techniques, such as a density-functional first-principles method [1.30], or a density-functional tight-binding method [1.31], where practical atomic structures are assumed for SiO_2 layers, as shown in Figure 1.9(b), have been applied to reveal large quantitative differences, in comparison with simulations of H-terminated Si film.

Furthermore, considering the sub-10 nm technology node, GAA nanowire MOSFET with ideal gate electrostatic controllability is attracting a lot of attention. Figure 1.10 shows the schematic of GAA nanowire MOSFET constructed from a diamond crystal, where a square-shaped cross-section is assumed. In nanowire MOSFETs with the channel length shorter than 10 nm, its cross-sectional dimensions are supposed to be less than 5 nm. Hence, the number of atoms in the cross-section becomes countable, as shown in Figure 1.10(a), (b) and (c).

Accordingly, the electronic states significantly depend on geometrical parameters such as wire orientation and cross-sectional dimension [1.32]. Moreover, not only electrons, but also phonons, are spatially confined to a nanometer scale [1.33, 1.34]. To deeply understand their behaviors, we need an atomistic device simulation technique based on a first-principles approach [1.35, 1.36], or a tight-binding approach [1.37, 1.38], if necessary coupled with phonon band structure calculation and electron-phonon interaction modeling [1.33, 1.34]. We will describe such a challenge in Chapters 2 and 6.

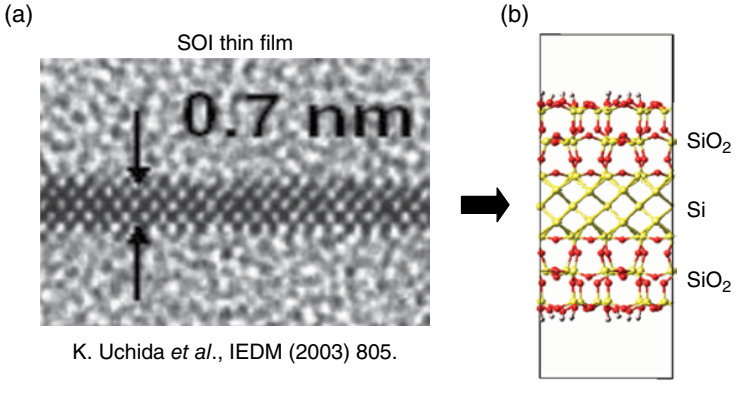

Figure 1.9 (a) Experimentally fabricated SOI-MOSFET with Si channel thickness of 0.7 nm, which corresponds to the 5-atomic-layer thickness of Si atoms [1.29]. (b) Example of SOI atomic structure used for *ab initio* simulations.

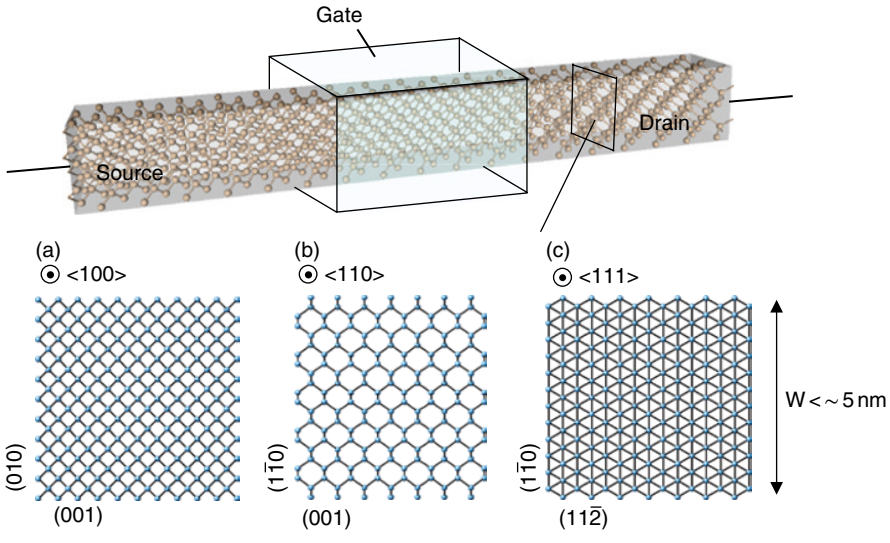

Figure 1.10 Schematic of GAA nanowire MOSFET constructed from a diamond crystal. As shown in the lower figures, when the cross-sectional dimensions are equal to or less than 5 nm, the number of atoms in the cross-section becomes countable, where the wire direction is (a) <100>-; (b) <110>-; and (c) <111>-orientations.

In summary, the introduction of new device structures and new channel materials are expected to improve the device performance of MOSFETs, without depending on conventional geometrical scaling. On the other hand, they can exhibit quite different features from conventional MOSFETs, because they are "new" technologies. Most of them are caused by quantum mechanical properties of carriers. In a sense, breaking the miniaturization limit of Si MOSFETs relies on the well-managed control of quantum mechanical effects and, therefore, the role of quantum mechanical simulation and atomistic analysis techniques will become more and more important than ever.

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2

First-principles Calculations for Si Nanostructures

A knowledge of the band structure of a material is the first necessary step to understanding and predicting its electronic properties. With the recent advancement in semiconductor microfabrication technologies, novel device architectures, coupled with nano-structures such as ultrathin films and nanowires, have been proposed. The band structure plays a fundamental role in determining both the electrostatics and the dynamics of carriers in those nano-structures. In this chapter, the band structures computed for Si nano-structures using first-principle density-functional theory are presented, and atomistic effects in Si nano-structures are discussed.

2.1 Band Structure Calculations

2.1.1 Si Ultrathin-body Structures

With aggressively downscaling to a nanometer scale of the VLSI technology, ultrathin-body (UTB) structures of Si, such as silicon-on-insulator (SOI) and FinFETs, are getting a lot of attention because of their superior immunity to short channel effects. Experimentally, extremely-scaled SOI-MOSFETs with Si channel thickness less than 1 nm were fabricated as shown in Figure 2.1, and fundamental device operation was successfully reported [2.1]. In such atomic-scale dimensions, not only the quantum confinement effects, but also the roles of interfaces between Si channel and gate oxides will be important. We here present our atomistic investigation on electronic properties of SOI channels, based on a first-principles simulation.

Figure 2.2 shows the atomic structures used in the Si-UTB simulations, where we employed three types of spatial confinement [2.2]. The SiO_2 layers were assumed to be crystalline and placed onto the Si (001) surfaces without any defects – that is, the Si/SiO_2 interfaces are geometrically abrupt. To apply the supercell technique, vacuum layers with a sufficient thickness are included above and below the structures. We refer to (a) and (b) as the silicon-on-insulator (SOI) model, and (c) as the H-terminated model, respectively.

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