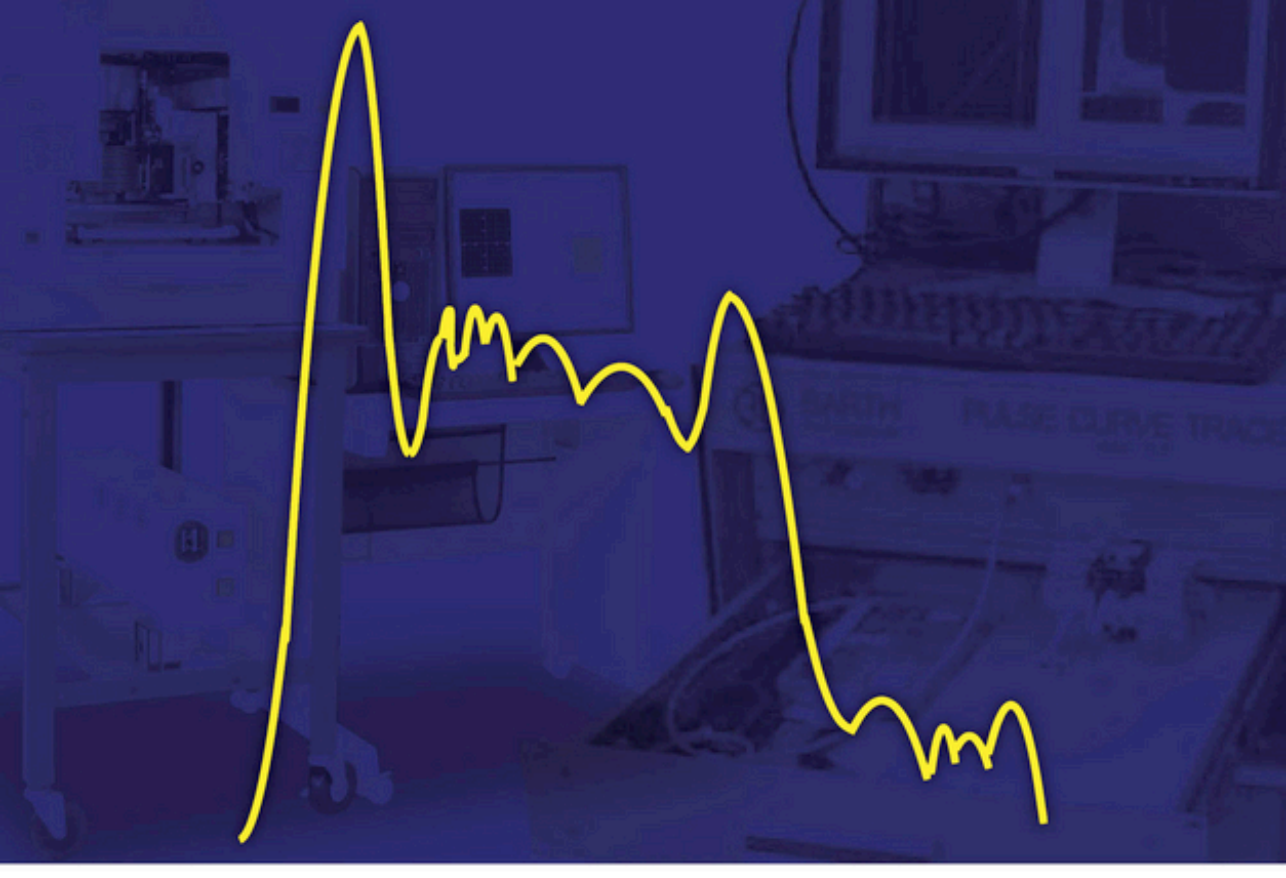

ESD Testing

FROM COMPONENTS TO SYSTEMS

STEVEN H. VOLDMAN

WILEY

ESD TESTING

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ESD TESTING
FROM COMPONENTS TO SYSTEMS

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IEEE Fellow, New York, USA

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To My Parents
Carl and Blossom Voldman

Contents

About the Author

Dr Steven H. Voldman is the first IEEE Fellow in the field of electrostatic discharge (ESD) for "Contributions in ESD protection in CMOS, Silicon on Insulator and Silicon Germanium Technology." He received his BS in Engineering Science from the University of Buffalo (1979); a first MS EE (1981) from Massachusetts Institute of Technology (MIT); a second degree EE Degree (Engineer Degree) from MIT; an MS Engineering Physics (1986); and a PhD in electrical engineering (EE) (1991) from University of Vermont under IBM's Resident Study Fellow program.

Voldman was a member of the semiconductor development of IBM for 25 years. He was a member of the IBM's Bipolar SRAM, CMOS DRAM, CMOS logic, Silicon on Insulator (SOI), 3D memory team, BiCMOS and Silicon Germanium, RF CMOS, RF SOI, smart power technology development, and image processing technology teams. In 2007, Voldman joined the Qimonda Corporation as a member of the DRAM development team, working on 70, 58, 48, and 32 nm CMOS DRAM technology. In 2008, Voldman worked as a full-time ESD consultant for Taiwan Semiconductor Manufacturing Corporation (TSMC) supporting ESD and latchup development for 45 nm CMOS technology and a member of the TSMC Standard Cell Development team in Hsinchu, Taiwan. In 2009–2011, Steve became a Senior Principal Engineer working for the Intersil Corporation working on analog, power, and RF applications in RF CMOS, RF Silicon Germanium, and SOI. In 2013–2014, Dr Voldman was a consultant for the Samsung Electronics Corporation in Dongtan, South Korea.

Dr Voldman was chairman of the SEMATECH ESD Working Group from 1995 to 2000. In his SEMATECH Working Group, the effort focused on ESD technology benchmarking, the first transmission line pulse (TLP) standard development team, strategic planning, and JEDEC-ESD Association standards harmonization of the human body model (HBM) Standard. From 2000 to 2013, as Chairman of the ESD Association Work Group on TLP and very-fast TLP (VF-TLP), his team was responsible for initiating the first standard practice and standards for TLP and VF-TLP. Steven Voldman has been a member of the ESD Association Board of Directors and Education Committee. He initiated the "ESD on Campus" program that was established to bring ESD lectures and interaction to university faculty and students internationally; the ESD on Campus program has reached over 40 universities in the United States, Korea, Singapore, Taiwan, Senegal, Malaysia, Philippines, Thailand, India, and China. Dr Voldman teaches short courses and tutorials on ESD, latchup, patenting, and invention.

He is a recipient of 258 issued US patents and has written over 150 technical papers in the area of ESD and CMOS latchup. Since 2007, he has served as an expert witness in patent litigation and has also founded a limited liability corporation (LLC) consulting business supporting

patents, patent writing, and patent litigation. In his LLC, Voldman served as an expert witness for cases on DRAM development, semiconductor development, integrated circuits, and ESD. He is presently writing patents for law firms. Steven Voldman provides tutorials and lectures on inventions, innovations, and patents in Malaysia, Sri Lanka, and the United States.

Dr Voldman also has written an article for *Scientific American* and is an author of the first book series on ESD, latchup, and EOS (nine books): *ESD: Physics and Devices*; *ESD: Circuits and Devices*; *ESD: RF Technology and Circuits*; *Latchup*; *ESD: Failure Mechanisms and Models*; *ESD: Design and Synthesis*; *ESD Basics: From Semiconductor Manufacturing to Product Use*; *Electrical Overstress (EOS): Devices, Circuits and Systems*; and *ESD: Analog Circuits and Design,* as well as a contributor to the book *Silicon Germanium: Technology, Modeling, and Design* and a chapter contributor to *Nanoelectronics: Nanowires, Molecular Electronics, and Nanodevices.* In addition, the International Chinese editions of book *ESD: Circuits and Devices*; *ESD: RF Technology and Circuits*; *ESD: Design and Synthesis*; and *ESD Basics: From Semiconductor Manufacturing to Product Use* are also released.

Preface

The book *ESD Testing: From Components to Systems* was targeted for the semiconductor process and device engineer, the circuit designer, the ESD/latchup test engineer, and the ESD engineer. In this book, a balance is established between the technology and testing.

The first goal of this book is to teach the ESD models used today. There are many ESD test models, and more types are being developed today and in the future.

The second goal is to show recent test systems and test standards. Significant change in both the test methodologies and issues are leading to proposal of new ESD models, introduction of new standards, and an impact on product diversity and product variety.

The third goal is to expose the reader to the growing number of new testing methodologies, concepts, and equipment. In this book, commercial test equipment is shown as an example to demonstrate the "state-of-the-art" of ESD testing. Significant progress has been made in recent years in ESD, EOS, and EMC.

The fourth goal, as previously done in the ESD book series, is to teach testing as an ESD design practice. ESD testing can be used as a design methodology or an ESD tool. ESD testing can lead to understanding of the fundamental practices of ESD design and the ESD design discipline. This practice uses ESD testing for "de-bugging" and diagnosis.

The fifth goal is to provide a book that can view the different test methods independently. Each chapter is independent so that the reader can study or read about a test model independent of the other test models.

The sixth goal is to provide a text where one can compare the interrelationship between one ESD model and another ESD model. In many cases, there is commonality between the test waveform, the test procedure, and even failure mechanisms.

The seventh goal is to provide a text structure similar to a standard or standard test method, but read easier than reading a standard document. The goal was also to reduce the level of details of the standard to simplify the understanding.

The book *ESD Testing: From Components to Systems* consists of the following:

Chapter 1 introduces the reader to fundamentals and concepts of the electrostatic discharge (ESD) models and issues.

Chapter 2 discusses the human body model (HBM). It discusses the purpose, scope, waveforms, test procedures, and test systems. In this chapter, both the wafer-level and

product-level test methodologies are discussed. This chapter includes HBM failure mechanisms to circuit solutions. Alternative test methodologies such as sampling and split fixture methods are reviewed.

Chapter 3 discusses the machine model (MM). It discusses the purpose, scope, waveforms, test procedures, and test systems. In this chapter, both the wafer-level and product-level test methodologies are discussed. This chapter includes MM failure mechanisms to circuit solutions. Alternative test methodologies such as the small charge model (SCM) are discussed. In addition, correlation relations of HBM to MM ratio are analyzed and reviewed.

Chapter 4 discusses the charged device model (CDM). It discusses the purpose, scope, waveforms, CDM test procedures, and CDM test systems. This chapter includes CDM failure mechanisms to circuit solutions to avoid CDM failures. Alternative test methodologies such as the socketed device model (SDM) and charged board model (CBM) are discussed.

Chapter 5 discusses the transmission line pulse (TLP) methodology and its importance in the semiconductor industry and ESD development. It discusses the purpose, scope, waveforms, TLP pulsed *I–V* characteristics, TLP test procedures, and TLP test system configurations. TLP current source, time domain reflection (TDR), time domain transmission (TDT), and time domain reflection and transmission (TDRT) configurations is explained

Chapter 6 discusses the very fast transmission line pulse (VF-TLP) methodology. It discusses the purpose, scope, waveforms, VF-TLP pulsed *I–V* characteristics, VF-TLP test procedures, and VF-TLP test system configurations. Alternative test methods such as ultra fast transmission line pulse (UF-TLP) are discussed.

Chapter 7 discusses the system-level method, known as IEC 61000-4-2. It discusses the purpose, scope, IEC 61000-4-2 waveforms, IEC 61000-4-2 table configurations, and requirements. Failure mechanisms and circuit solutions to avoid failures are explained.

Chapter 8 discusses the human metal model (HMM) method. The HMM model has many similarities to the system-level method, known as IEC 61000-4-2. It discusses the purpose, scope, waveforms, HMM table configurations, and requirements as well as the distinctions and commonality to the IEC 61000-4-2 test method.

Chapter 9 discusses the system-level transient surge method, known as IEC 61000-4-5. It discusses the purpose, scope, IEC 61000-4-5 waveforms, IEC 61000-4-5 table configurations, and requirements. Failure mechanisms and circuit solutions to avoid failures are explained. The distinction from the IEC 61000-4-2 is highlighted.

Chapter 10 discusses the cable discharge event (CDE) method. It discusses the purpose, scope, waveforms, cable configurations, and impact on the pulse event. Examples of cable-induced failures are given, as well as circuit- and system-level solutions to avoid chip and system failures.

Chapter 11 discusses latchup. It addresses latchup testing, characterization, and design. It also addresses latchup test techniques for product-level testing. Technology benchmarking to ground rule development is also briefly discussed.

Chapter 12 discusses electrical overstress (EOS). It focuses on electrical and thermal safe operating area (SOA) and how EOS occurs. It also focuses on how to distinguish latchup from EOS events.

Chapter 13 discusses electromagnetic compatibility (EMC). It addresses ESD and EMC testing and characterization methods. It also serves as a brief introduction to this large subject matter.

Hopefully, the book covers the trends and directions of ESD testing discipline.
Enjoy the text, and enjoy the subject of ESD testing.

B”H
Steven H. Voldman
IEEE Fellow

Acknowledgments

I would like to thank the individuals who have helped me learn about experimental work, high current testing, high voltage testing, electrostatic discharge (ESD) testing, electrical overstress (EOS), and standards development. In the area of ESD, EOS, and latchup testing, I would like to thank for all the support received from SEMATECH, the ESD Association, and the JEDEC organizations.

I would like to thank the SEMATECH organization for allowing me to establish the SEMATECH ESD Work Group: this work group initiated the ESD technology benchmarking test structures, the JEDEC-ESD Association collaboration on ESD standard development, alternate test methods, and most important, the initiation of the transmission line pulse (TLP) standard development.

I thank the ESD Association ESD Work Group (WG) standard committees for many years of discussion on standard developments and on human body model (HBM), machine model (MM), charged device model (CDM), cable discharge event (CDE), human metal model (HMM), TLP testing, and very fast transmission line pulse (VF-TLP) testing. I also thank the ESD Association Standards Development Work Group 5.5 TLP testing committee. We were very fortunate to have a highly talented and motivated team to rapidly initiate the TLP and VF-TLP documents for the semiconductor industry; this included for the development of the TLP and VF-TLP standards, which was a significant accomplishment that has influenced the direction of ESD testing. I am thankful to my colleagues Robert Ashton, Jon Barth, David Bennett, Mike Chaine, Horst Gieser, Evan Grund, Leo G. Henry, Mike Hopkins, Hugh Hyatt, Mark Kelly, Tom Meuse, Doug Miller, Scott Ward, Kathy Muhonen, Nathaniel Peachey, Jeff Dunihoo, Keichi Hasegawa, Jin Min, Yoon Huh, and Wei Huang. I am also thankful to Tze Wee Chen of Stanford University for discussions on the ultra-fast transmission line pulse (UF-TLP) testing.

I am grateful to the Oryx Instrument ESD test development team for years of ESD test support and the Thermo Fisher Scientific team of David Bennett, Mike Hopkins, Tom Meuse, Tricia Rakey, and Kim Baltier. My sincere thanks goes to Jon Barth of Barth Electronics for usage of the images of the Barth test equipment for this text; Keichi Hasegawa of Hanwa Electronics for the images of the Hanwa test equipment; Yoon Huh and Jin Min of Amber Precision Instruments for the scanning images and the test equipment; Wei Huang for the images of the ESDEMC test equipment; Jeff Dunnihoo of Pragma Design Inc for the current reconstruction method images; the HPPI corporation for images of its TLP test equipment; and Chris O'Connor of UTI Inc. for transient latchup analysis.

I would like to thank the JEDEC organization's ESD committee.

This work was supported by the institutions that allowed me to teach and lecture at conferences, symposiums, industry, and universities; this gave me the motivation to develop the texts. I would like to thank for the years of support and the opportunity to provide lectures, invited talks, and tutorials at the International Physical and Failure Analysis (IPFA) in Singapore, the Electrical Overstress/Electrostatic Discharge (EOS/ESD) Symposium, the International Reliability Physics Symposium (IRPS), and the Taiwan Electrostatic Discharge Conference (T-ESDC), International Conference on Solid State and Integrated Circuit Technology (ICSICT), and ASICON.

Finally, I am immensely thankful to the ESD Association office for the support in the area of publications, standards developments, and conference activities – Lisa, Christine, and Terry. I also thank the publisher and staff of John Wiley and Sons, for including the text *ESD Testing: From Components to Systems* as part of the ESD book series.

To my children, Aaron Samuel Voldman and Rachel Pesha Voldman, good luck to both of you in the future.

And Betsy H. Brown, for her support on this text …

And of course, my parents, Carl and Blossom Voldman.

B"H
Dr Steven H. Voldman
IEEE Fellow

1

Introduction

1.1 Testing for ESD, EMI, EOS, EMC, and Latchup

In the electronics industry, testing of components and systems is a part of the process of qualifying and releasing products. Standards are established to provide methodology, process, and guidance to quantify the technology issue [1–14]. Testing is performed to evaluate the sensitivity and susceptibility of products to electric, magnetic, and electromagnetic events. These can be categorized into electrostatic discharge (ESD) [1–12], electrical overstress (EOS), electromagnetic interference (EMI), and electromagnetic compatibility (EMC) events, and latchup (Figure 1.1) [13]. In the electronic industry, tests and procedures have been established to quantify the influence of these events on components and systems associated with ESD, EOS, EMC, and latchup [15–24].

1.2 Component and System Level Testing

In the testing of electronics, different tests and procedures were established that tested components, and other tests for testing of systems. These tests have been established based on the environment that the components and systems experience in processing, assembly, shipping, to product use [1–24].

Figure 1.2 shows examples of component tests that are applied to wafer level, packaged and unpackaged products. Today, it is common to test semiconductor components for the following standards. These include the human body model (HBM) [1], machine model (MM) [2, 3], charged device model (CDM) [4, 5], to transmission line pulse (TLP) [6, 7], and very fast transmission line pulse (VF-TLP) [8, 9]. In the future chapters, these tests are discussed in depth.

Figure 1.3 shows examples of system level tests that are applied to systems to address the robustness to environments that the systems may experience in product use. For system level tests, it is now common to test for the IEC 61000-4-2 [10], human metal model (HMM) [11], IEC 61000-4-5 [12], and cable discharge events (CDE).

ESD Testing: From Components to Systems, First Edition. Steven H. Voldman.

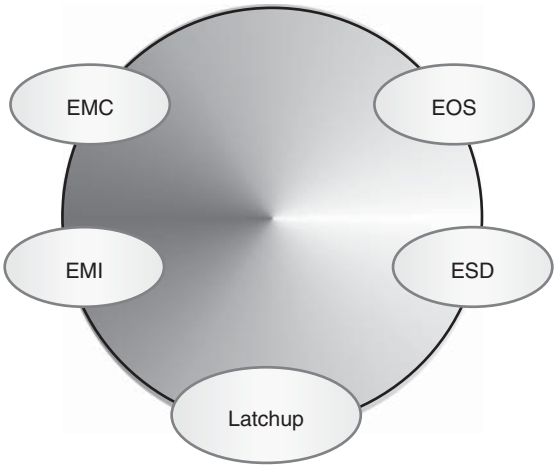

Figure 1.1 ESD, EMI, EOS, and EMC

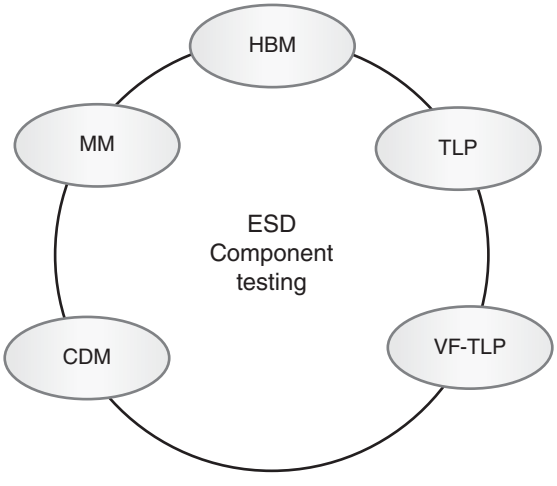

Figure 1.2 Component tests

1.3 Qualification Testing

Many of the tests are used for different purposes. Some electrical tests are established for characterization, whereas other tests have been established for qualification of components or systems. Qualification tests are performed to guarantee or insure quality and reliability in the system, or in the field. Figure 1.4 shows examples of qualification tests that are performed in the electronic industry. These qualification tests include standard practice (SP) documents, to standard test method (STM).

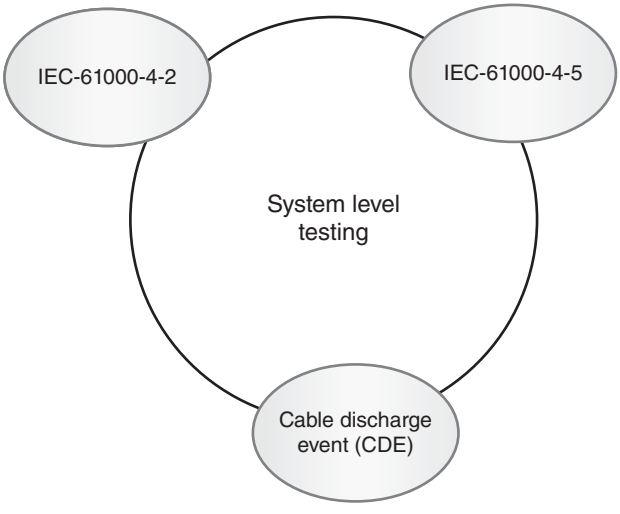

Figure 1.3 System level tests

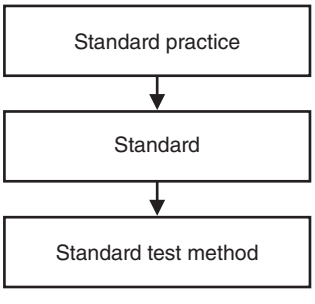

Figure 1.4 Qualification testing

1.4 ESD Standards

In the development of these qualification processes, different types of documents and processes are established. In standards development, practices and processes are established for the quality, reliability, and release of products to customers.

1.4.1 Standard Development – Standard Practice (SP) and Standard Test Methods (STMs)

In the development of these qualification processes, a standard practice is established for testing of components and systems. A standard practice (SP) is a procedure or process that is

established for testing. The document for the standard practice is called the standard practice (SP) document. A second practice is to establish an STM. The distinction between the standard practice (SP) and an STM is the STM procedure insures reproducibility and repeatability. In standards development, both standard practices (SP) and STM are established for the quality, reliability, and release of products to customers.

1.4.2 Repeatability

In STM development, repeatability is an important criterion in order to have a process elevate from a standard practice to an STM. It is important to know that if a test is performed, the experimental results are repeatable (Figure 1.5).

1.4.3 Reproducibility

In STM development, reproducibility is a second important criterion in order to have a process elevate from a standard practice (SP) to an STM. Reproducibility is key to verify that the experimental results can be reproduced (Figure 1.6).

1.4.4 Round Robin Testing

In order to determine if a standard practice can be elevated to an STM, reproducibility and repeatability are evaluated in a process known as Round Robin (RR) process. Statistical analysis is initiated to determine the success or failure of reproducibility and repeatability as part of the experimental methodology. RR is an interlaboratory test that can include measurement, analysis or performing an experiment. This process can include a number of

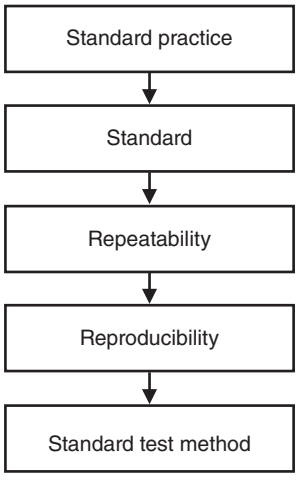

Figure 1.5 Repeatability and Reproducibility

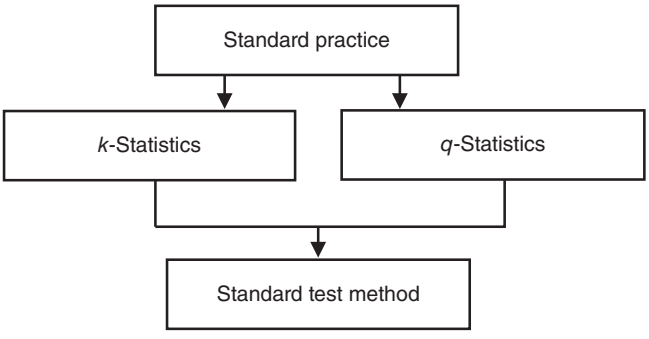

Figure 1.6 SP to STM Process

independent scientists and independent laboratories. In the case of ESD and EOS testing, different commercial test equipment is used in the process. To assess the measurement system, the statistics of analysis of variance (ANOVA) random effects model is used.

1.4.5 Round Robin Statistical Analysis – k-Statistics

In the RR process, the within-laboratory consistency statistics is known as the *k*-statistics. The *k*-statistics is the quotient of the laboratory standard deviation and the mean standard deviation of all the laboratories. These can be visualized using Mandel statistics and Mandel plots. Mandel's *k* is an indicator of the precision compared to the pooled standard deviation across all groups. Mandel's *k* plot is represented by a bar graph (Figure 1.7).

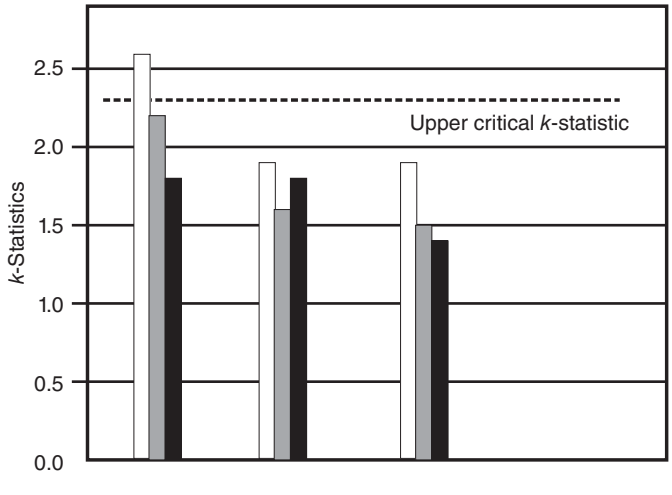

Figure 1.7 Mandel *k*-statistics plot

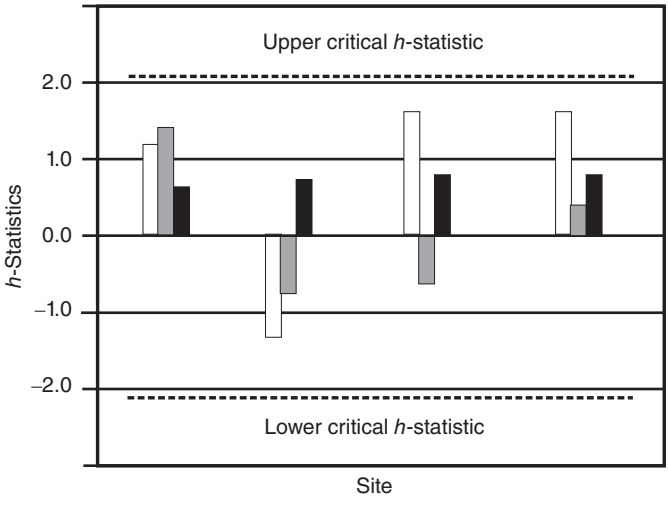

Figure 1.8 Mandel *h*-statistics plot

1.4.6 Round Robin Statistical Analysis – h-Statistics

In the RR process, the between-laboratory consistency statistics is known as the *h*-statistics. The *h*-statistics is the ratio of the difference between the laboratory mean and the mean of all the laboratories, and the standard deviation of the means from all the laboratories. These can be visualized using Mandel statistics and Mandel plots. Mandel's statistics are traditionally plotted for interlaboratory study data, grouped by laboratory to give a graphical view of laboratory bias and precision. Mandel's *h*-plots are bar graphs around a zero axis (Figure 1.8).

1.5 Component Level Standards

Today, in the semiconductor industry, components are tested to the HBM, MM, and CDM [1–5]. These tests are traditionally done on packaged components. In these tests, the components are also unpowered. For the qualification of semiconductor components for over 20 years, the HBM, MM, and CDM tests were completed prior to shipping components to a customer or system developer. In addition, latchup qualification was required in the shipping of components since the 1980s time frame [13]. A new test of components includes the HMM test to evaluate the influence of the components on system level tests.

In the 1990s, TLP testing became popular and is now a common characterization practice in the semiconductor industry. TLP testing did not have an established methodology until the year 2003 [6]. TLP testing is performed on test structures, circuits, to components. This was followed by a second test method known as the VF-TLP testing method [8]. VF-TLP testing is also completed on test structures to components. These TLP tests can also be performed on systems.