# Electronic Engineering and Information Science

Edited by
Jinghua Yin, Bo Su and Dongxing Wang

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*Edited by*

**Jinghua Yin, Bo Su and Dongxing Wang**

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# Preface

2014 International Conference of Electronic Engineering and Information Science (ICEEIS 2014) will be held 21-22 June in Harbin, China. The ICEEIS 2014 is sponsored by Harbin University of Science and Technology.

The main role of ICEEIS 2014 is to bring together innovators from engineering researchers, scientists, practitioners to provide a forum to discuss ideas, concepts, and experimental results related to all aspects of electronic engineering and information science. In order to meet high standard of TTP, Advanced Materials Research, the organization committee has made their efforts to do the following things. Firstly, poor quality papers have been refused after reviewing course by anonymous referee experts. Secondly, periodically review meetings have been held around the reviewers about six times for exchanging reviewing suggestions. Finally, the conference organization had several preliminary sessions before the conference. Through efforts of different people and departments, the conference will be successful and fruitful.

ICEEIS 2014 is co-sponsored by Harbin University. In addition, the conference organizer will invite some keynote speakers to deliver their speech in the conference. All participants will have chance to discuss with the speakers face to face, which is very helpful for participants.

We hope that you will enjoy the conference and find the ICEEIS 2014 exciting. We are looking forward to seeing more friends at the next conference.

Jinghua Yin

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# Phasor Analysis Based Fault Modeling and Fault Diagnosis Methods for Linear Analog Circuits

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**Keywords:** Analog Fault Diagnosis, Fault modeling, Fault Feature, Tolerance.

**Abstract.** Soft fault diagnosis and tolerance are two challenging problems in linear analog circuit fault diagnosis. To solve these problems, a phasor analysis based fault modeling method and its theoretical proof are presented at first. Second, to form fault feature data base, the differential voltage phasor ratio (DVPR) is decomposed into real and imaginary parts. Optimal feature selection method and testability analysis method are used to determine the optimal fault feature data base. Statistical experiments prove that the proposed fault modeling method can improve the fault diagnosis robustness. Then, Multi-class support vector machine (SVM) classifiers are used for fault diagnosis. The effectiveness of the proposed approaches is verified by both simulated and experimental results.

## Introduction

The catastrophic faults are handled in Ref.[4]. Methods proposed in literatures [5], [6] are used to diagnosis discretized parameter faults. Both catastrophic and discretized parameter fault diagnosis problem are discussed in papers [7]. Local spot defect is handled in reference [8]. The author also point out that the local spot defect are often modeled by open and short circuits. Aiming at linear Switched-Capacitor Circuit fault, Hao-Chiao Hong [9] proposes a static linear behavior modeling method. By using this method, the CUT is partitioned into several functional macros. Each functional macro has specified design parameters which constitute the parameter set and determine the transfer function of the CUT. If frequency responses are out of the design specification, the parameter set is supposed to be faulty. This method falls into functional test method.

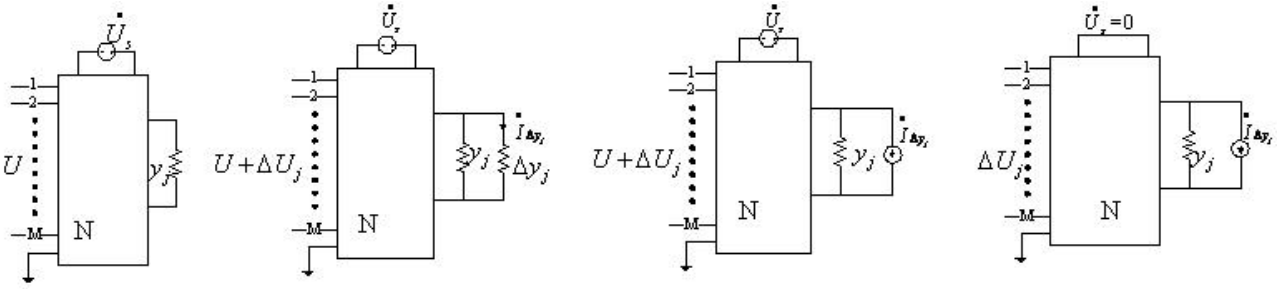
A high level fault modeling method proposed in Ref.[10] is used to model transistor level analog faults. In Ref. [11], a node-voltage sensitivity sequence dictionary method is established. Whether a fault is hard or soft, only one fault characteristic code is needed to detect any fault of a component. Based on the ideas in Ref.[11], Ref.[12] and [13] developed methods for diagnosing soft faults of tolerance analog circuits and nonlinear circuits. A slope fault feature based soft fault diagnosis method is proposed in Ref.[14]. It is a uniform fault modeling method for both hard and soft fault in linear circuit. By using fuzzy math to replace ambiguity sets to handle tolerance issue, Wang and Yang [15] propose an equivalent faults model to handle test node selection problem. However, all the mentioned methods do not model fault on complex domain, and do not handle tolerance well.

This paper focuses on component level fault modeling and fault diagnosis problem. First, the modeling idea is to establish the relationship between the DVPR and fault component by using phasor analysis. This kind of relationship is independent from the value of fault component and can be served as fault feature. The feature can be easily obtained by using simulation. Second, the optimal test selection method proposed in [16] are used to determine the optimal fault feature data

base. Based on this data base, Multi-class SVM classifiers are trained and used to future fault diagnosis.

**Principle of The Proposed Fault Model**

*A. Theoretical Foundation*




(a) (b) (c) (d)

Fig. 1 (a): Nominal Network N (b): Fault Network N+ΔN (c): Equivalent Fault Network (d): Differential NetworkΔN

Suppose that CUT $N$ shown in Fig.1(a) is a linear time-invariant passive circuit. The admittance of passive element is $y_j$.$\dot{U}$ is voltage phasor vector of measurable nodes{1, 2……M} in $N$. $\dot{U}_s$ is independent source. Without loss of generality, assume that the admittance is shifted to $y_j + \Delta y_j$ when a fault occurs to $x_j$. As a result, the fault voltage phasor vector of measurable nodes is $\dot{U}+\Delta\dot{U}_j$. Suppose that the current in $\Delta y_j$ is $\dot{I}_{\Delta y_j}$, according to the substitution theorem **[**16], the passive element $\Delta y_j$ can be replaced with independent current source $\dot{I}_{\Delta y_j}$, as shown in Fig. 1(c). According to the superposition theorem **[**16], the voltage vector on measurable nodes in Fig. 1(c) equals the algebraic sum of the responses caused by $\dot{U}_s$ and $\dot{I}_{\Delta y_j}$ acting alone. Fig. 1(a) shows that $\dot{U}_s$ acts alone, and Fig. 1(d) shows that $\dot{I}_{\Delta y_j}$ acts solely. In Fig.1(d)

$$\Delta\dot{U}_j = Z_j \dot{I}_{\Delta y_j} \tag{1}$$

where $Z_j$ is the transfer impedance vector from fault port to measurable nodes. It can be seen from this figure that $Z_j$ is independent from the value of $\dot{I}_{\Delta y_j}$; hence, it is independent from the fault magnitude $\Delta y_j$. Additionally, $Z_j$ is uniquely determined by the nominal CUT and the location of fault component. Totally, there are M measurable nodes in Fig. 1(a). Hence, vector $\Delta\dot{U}_j$ can be obtained. By using $\Delta\dot{U}_{1j}$ to divide $\Delta\dot{U}_j$, differential voltage phasor ratio (DVPR) vector $k_j$ is obtained.

$$k_j = \frac{\Delta \dot{U}_j}{\Delta \dot{U}_{1j}} = \begin{pmatrix} 1 \\ Z_{2j}/Z_{1j} \\ Z_{3j}/Z_{1j} \\ \vdots \\ Z_{Mj}/Z_{1j} \end{pmatrix} = \begin{pmatrix} k_{1j} \\ k_{2j} \\ k_{3j} \\ \vdots \\ k_{Mj} \end{pmatrix}. \tag{2}$$

Obviously, $k_j$ is uniquely determined by $Z_j$; hence, it is uniquely determined by the nominal CUT and the location of fault component $y_j$. Hence, $k_j$ can act as fault feature of $y_j$. More importantly, $k_j$ is independent from the fault magnitude of $y_j$. Regardless of what kind of fault it is and how much the fault magnitude is, $k_j$ are fixed. It is a uniform fault feature for both hard (open or short) and soft (parametric) faults. Based on formula (2), the following simulation steps are proposed to calculate $k_j$.

*B. Simulation Based Fault Model Acquisition*

From formula (2), the vector $k_j$ is calculated by using following equation.

$$k_j = \frac{\Delta \dot{U}_j}{\Delta \dot{U}_{1j}}. \tag{3}$$

Based on this formula and Fig. 1(b), the vector $k_j$ can be computed by using following simulation steps.

Step 1) The CUT is stimulated by independent source $\dot{U}_s$. Fault free voltage $\dot{U}$ on measurable nodes is stored.

Step 2) Component $y_j$ is randomly adjusted to any value other than fault free. Voltage on measurable nodes is recorded as $\dot{U}_j$.

Step 3) Calculating differential voltage $\Delta \dot{U}_j = \dot{U}_j - \dot{U}$. $k_j$ is calculated by using (3).

*C. Construction of the Optimal Fault Database*

If there are *N* potential fault components in the CUT, the DVPR $K$ is a M×N matrix. In this matrix, columns represent different fault sources and the rows show the available test nodes. There might be identical columns in matrix $K$, viz., $k_i = k_j \left(i \neq j\right)$. It means that the corresponding fault sources have the same fault feature. Faults with the same fault feature form an ambiguity set. Identical rows represent redundant test nodes. The test nodes selection algorithm proposed in [16] is used to select optimal test nodes.

Based on equation (2), $k_{1j} = 1$. Hence, all the elements in the first row of matrix $K$ is equal to 1. It means that the first test node cannot distinguish any fault. This row should be removed from matrix $K$. Due to that impedance $Z_j$ is complex vector, $k_{ij} = Z_{ij}/Z_{1j}$ is complex number too. Suppose that the real and imaginary parts of $k_{ij}$ are $\mathrm{Re}\,k_{ij}$ and $\mathrm{Im}\,k_{ij}$ respectively. A matrix $\tilde{K}$ derived from $K$ is as follows.

$$\tilde{K}=\begin{bmatrix}\tilde{k}_1 & \tilde{k}_2 & \cdots & \tilde{k}_N\end{bmatrix}=\begin{bmatrix}\mathrm{Re}\,k_{21} & \mathrm{Re}\,k_{22} & \cdots & \mathrm{Re}\,k_{2N}\\ \mathrm{Im}\,k_{21} & \mathrm{Im}\,k_{22} & \cdots & \mathrm{Im}\,k_{2N}\\ \mathrm{Re}\,k_{31} & \mathrm{Re}\,k_{32} & \cdots & \mathrm{Re}\,k_{3N}\\ \mathrm{Im}\,k_{31} & \mathrm{Im}\,k_{32} & \cdots & \mathrm{Im}\,k_{3N}\\ \vdots & \vdots & \vdots & \vdots\\ \mathrm{Re}\,k_{M1} & \mathrm{Re}\,k_{M2} & \cdots & \mathrm{Re}\,k_{MN}\\ \mathrm{Im}\,k_{M1} & \mathrm{Im}\,k_{M2} & \cdots & \mathrm{Im}\,k_{MN}\end{bmatrix}. \tag{4}$$

where $\tilde{k}_j \in R^{2(\mathrm{M}-1)}$ is column vector, and fault feature database $\tilde{K}$ is $2(M-1)\times N$ matrix. $M$ is the number of optimal test nodes, and $N$ is the number of representative faults.

**SVM Classifier Based Fault Diagnosis**

In an actual analog circuit, a parameter of a circuit element may vary within a range around its nominal value without treating it as a fault. This is termed as "tolerance." Hence, when a fault occurs to circuit element $y_i$, the measured fault feature $\tilde{k}_f$ may not be equal to the nominal fault feature $\tilde{k}_i$ exactly. Under this circumstance, fault diagnosis is much more a fault classification problem. Support Vector Machine (SVM) is a powerful solution to the classification problems [18]. The simplest linear SVM classifier is adopted in this paper.

Step1) The fault free CUT is simulated, and the voltage vector on $M$ selected test nodes $\dot{U}$ is stored. The number of Monte Carlo simulation $N_M$ is preset.

Step 2) Suppose that there are $N$ representative fault components. For every representative fault component $y_j$, the following simulations are run for $N_M$ times.

Step2.1) The faulty parameter $\Delta y_j \in (0, (1-a)y_j) \cup ((1+a)y_j, \infty)$ is randomly generated by computer, where $a$ is the tolerance limit.

Step2.2) Within the tolerance range $((1-a)y_i,(1+a)y_i)$, all other fault free components' parameters are randomly generated by computer too.

Step2.3) The simulated fault voltage vector is recorded as $\dot{U}_f$.

Step 2.4) The differential voltage is $\Delta\dot{U}_i = \dot{U}_f - \dot{U}$. Fault feature $\tilde{k}_j \in R^{2(\mathrm{M}-1)}$ is calculated by using formula (2) and (4).

Step 3) The training data is $\{\tilde{k}_j, y_j\}$, $j=1,\cdots N_M \times N$, $y_j \in \{-1,1\}$, $\tilde{k}_j \in R^{2(\mathrm{M}-1)}$. There are $N$ representative fault components; hence, the training data is classified into $N$ groups, and $N(N-1)/2$ individual SVM networks are trained.

Totally, there are three phases in the proposed fault modeling and diagnosis procedure. The first phase includes fault modeling, testability analysis and fault feature database optimization. Fault modeling is to establish the optimal fault feature database $\tilde{K}$. The second phase is Multi-class SVMs training. All the involved simulations are executed by using Pspice under the supervision of Matlab. Except for the Monte Carlo simulations, all the faulty parameters are set by Matlab. Hence, the whole simulation process is automatically accomplished. The third phase is fault diagnosis. In

this phase, the trained Multi-class SVM classifiers are used to classify the simulated or actual fault data. All the algorithm and data process are realized by using Matlab.

## Experimental Results

In this section, not only the tolerance but also measurement error is taken into consideration. The following parameters are used in all the experiments.

—resistance tolerance limit $a_R$=±5%;

—capacitance tolerance limit $a_C$ =±10%;

—measurement error limit $e$=±5%.

The CUT is shown in Fig.2. Totally, there are six available test nodes. The first phase is fault modeling and fault feature database optimization. The CUT is stimulated by a 1-kHz 1-V sinusoidal wave. The simulated faulty and fault free voltage vector $\dot{U}$ are recorded in Table 1. Due to page limitation, only parts of the results are listed.

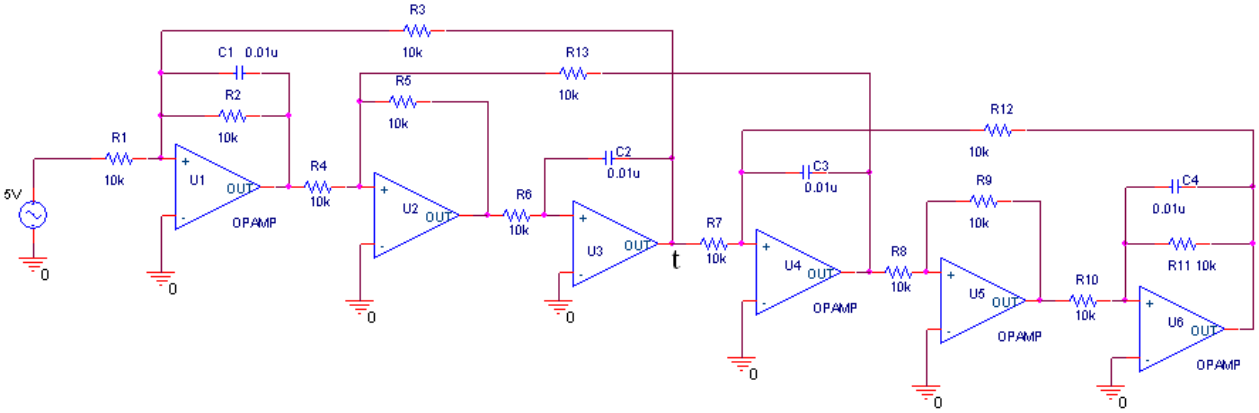



Fig.2. Leapfrog filter

Table 1 Simulated voltage vector (in volt)

| | Fault free | R1=5[kΩ] | R2=[5kΩ] | … | C3=10[nF] | C4=5[nF] | … | U5 fail | U6 fail |
|---|---|---|---|---|---|---|---|---|---|
| | $\dot{U}$ | $\dot{U}_1$ | $\dot{U}_2$ | … | $\dot{U}_{16}$ | $\dot{U}_{17}$ | … | $\dot{U}_{22}$ | $\dot{U}_{23}$ |
| n1 | -0.5262 - 0.0504$i$ | -1.0525 - 0.1007i | -0.3455 - 0.0216i | … | -0.6431 + 0.1150i | -0.5802 - 0.1029i | … | -0.3757- 0.1645i | -0.4380- 0.1857i |
| n2 | 0.4788+ 0.6351$i$ | 0.9576 + 1.2703i | 0.3271 + 0.4054i | … | 0.3633 + 0.3577i | 0.5874 + 0.6088i | … | 0.5034+ 0.9145i | 0.5792+ 0.8529i |
| n3 | -0.5054+ 0.3810$i$ | -1.0108 + 0.7620i | -0.3226 + 0.2603i | … | -0.2847 + 0.2891i | -0.4845 + 0.4675i | … | -0.7277+ 0.4006i | -0.6787+ 0.4609i |
| n4 | 0.0474- 0.5848$i$ | 0.0949 - 1.1695i | 0.0184 - 0.3838i | … | 0.2798 - 0.4727i | -0.0072 - 0.5059i | … | -0.1277- 0.7500i | -0.1413- 0.6672i |
| n5 | -0.0474+ 0.5848$i$ | -0.0949 + 1.1695i | -0.0184 + 0.3838i | … | -0.2798 + 0.4727i | 0.0072 + 0.5059i | … | 0.0639+ 0.3750i | 0.1413+ 0.6672i |
| n6 | -0.2294- 0.4406$i$ | -0.4588 - 0.8812i | -0.1597 - 0.2834i | … | -0.0123 - 0.4649i | -0.1512 - 0.4584i | … | -0.2147- 0.2401i | -0.1597- 0.2834i |

Based on the data shown in Table 1, the DVPRs are calculated. The results are saved in Table 2. The optimized fault features are shown in Table 3. It can be seen from this table that there are six ambiguity sets. The first component in each set is selected as representative. By using the optimization method proposed in former section, features on nodes $n2$, $n5$ and $n6$ are selected to diagnose fault.

Table 2 DVPR vector kj

| | R1 | R2 | … | C3 | C4 | … | U5 fail | U6 fail |
|---|---|---|---|---|---|---|---|---|
| | $k_1$ | $k_2$ | … | $k_{16}$ | $k_{17}$ | … | $k_{22}$ | $k_{23}$ |
| n1 | 1 | 1 | … | 1 | 1 | … | 1 | 1 |
| n2 | -1.0161-1.1097i | -1.0161-1.1097i | … | -0.7896+1.2566i | -0.7896+1.2566i | … | -0.7896+1.2566i | -0.7896+1.2566i |
| n3 | 0.8831-0.8086i | 0.8831-0.8086i | … | -1.0000-0.6283i | -1.0000-0.6283i | … | -1.0000-0.6283i | -1.0000-0.6283i |
| n4 | 0.0161+1.1097i | 0.0161+1.1097i | … | -0.2104-1.2566i | -0.2104-1.2566i | … | -0.2104-1.2566i | -0.2104-1.2566i |
| n5 | -0.0161-1.1097i | -0.0161-1.1097i | … | 0.2104+1.2566i | 0.2104+1.2566i | … | 1.1401-0.5289i | 0.2104+1.2566i |
| n6 | 0.5114+0.7884i | 0.5114+0.7884i | … | -0.7170-0.8062i | -0.5791+0.8928i | … | -0.5791+0.8928i | -0.5791+0.8928i |

Table 3 Optimal fault feature

| | | ***R1***,R2,R3,C1,U1 | ***R4***,R5,R13,U2 | ***R6***,C2,U3 | ***R7***,R12,C3,U4 | ***R8***,R9,U5 | ***R10***,R11,C4,U6 |
|---|---|---|---|---|---|---|---|
| | | $\tilde{k}_1$ | $\tilde{k}_2$ | $\tilde{k}_3$ | $\tilde{k}_4$ | $\tilde{k}_5$ | $\tilde{k}_6$ |
| n2 | Real part | -1.0161 | -0.7896 | -2.0512 | -0.7896 | -0.7896 | -0.7896 |
| | ***Imaginary part*** | ***-1.1097*** | ***1.2566*** | ***0.3056*** | ***1.2566*** | ***1.2566*** | ***1.2566*** |
| n5 | Real part | -0.0161 | -1.0512 | -1.0512 | 0.2104 | 1.1401 | 0.2104 |
| | ***Imaginary part*** | ***-1.1097*** | ***0.3056*** | ***0.3056*** | ***1.2566*** | ***-0.5289*** | ***1.2566*** |
| n6 | Real part | 0.5114 | 0.6160 | 0.6160 | -0.7170 | -0.5791 | -0.5791 |
| | ***Imaginary part*** | ***0.7884*** | ***-0.6926*** | ***-0.6926*** | ***-0.8062*** | ***0.8928*** | ***0.8928*** |

It can be seen from Table 3 that fault feature $\tilde{k}_j \in R^6$. The second phase is Multi-class SVMs training. Totally, 6(6−1)/2=15 individual SVM networks are needed to classify 6 ambiguity sets. For each representative component $y_j$, Monte Carlo simulation is run for 80 iterations. In each iteration, its faulty parameter is randomly generated within the range of $(0, 0.9y_j) \cup (1.1y_j, \infty)$. At the same time, all other components' parameter is randomly generated within the tolerance limit. Based on the simulated features $\tilde{k}_j \in R^6$, the Multi-class SVM classifiers are trained. The results, viz., weight vectors $\boldsymbol{w_j}$ and bias $b$, are shown in Table 4.

Table 4 Multi-class SVM training results

| | (R1,R4) | (R1,R6) | … | (R1,R10) | (R4,R6) | … | (R4,R10) | (R6,R7) | … | (R6,R10) | (R7,R8) | (R7,R10) | (R8,R10) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\boldsymbol{w_1}$ | $\boldsymbol{w_2}$ | … | $\boldsymbol{w_5}$ | $\boldsymbol{w_6}$ | … | $\boldsymbol{w_9}$ | $\boldsymbol{w_{10}}$ | … | $\boldsymbol{w_{12}}$ | $\boldsymbol{w_{13}}$ | $\boldsymbol{w_{14}}$ | $\boldsymbol{w_{15}}$ |
| ***w*** | -0.1298 | 0.2826 | … | -0.0455 | 1.1511 | … | 0.0530 | -0.4834 | … | -0.3402 | 0.0763 | 0.1376 | -0.1382 |
| | -0.5522 | -0.4724 | … | -0.4621 | 0.9577 | … | 0.0123 | -0.3478 | … | -0.2713 | -0.1902 | -0.2186 | 0.2339 |
| | 0.1948 | 0.3013 | … | -0.0705 | -0.1511 | … | -0.4550 | -0.4518 | … | -0.3227 | -0.4154 | 0.2311 | 0.6444 |
| | -0.3151 | -0.4874 | … | -0.4584 | -0.1090 | … | -0.3454 | -0.3535 | … | -0.2450 | 0.6479 | -0.3237 | -0.9906 |
| | 0.0048 | 0.0074 | … | 0.1749 | 0.0890 | … | 0.3947 | 0.4548 | … | 0.2799 | 0.0208 | -0.0357 | -0.2550 |
| | 0.3097 | 0.4791 | … | -0.0819 | 0.0064 | … | -0.6508 | 0.0519 | … | -0.4616 | -0.6452 | -1.3881 | -0.2492 |
| b | -0.0618 | 0.2864 | … | 0.1239 | 0.6568 | … | 0.1834 | -0.1739 | … | -0.1339 | 0.3968 | 0.8128 | -0.3997 |

Fault diagnosis is realized by using the training results shown in Table 4. In actual application, the accuracy of the proposed fault diagnosis method is affected by the tolerance problem and measurement error. To check the accuracy, statistical simulations are carried out. For each representative fault component, its fault range is classified into three ranges.

$$R_f = \begin{cases} (0.8R_0, 0.9R_0) \cup (1.1R_0, 1.2R_0) \\ (0.7R_0, 0.8R_0) \cup (1.2R_0, 1.3R_0) \\ (0, 0.7R_0) \cup (1.3R_0, \infty) \end{cases} \quad (5)$$

where $R_f$ is the fault parameter and $R_0$ represents fault free parameter. Within each fault range, simulation is run for 100 iterations. Faulty parameter is randomly generated within the predefined fault range. The other components are varied within the tolerance limit. Because there are six representative faults; hence, there are 6×3×100=1800 simulations, and there are 1800 fault features to be diagnosed. Random measurement errors are added to fault voltage vectors, and the fault features are calculated. Classifiers shown in Table 4 are used to diagnosis faults. The results are shown in Table 5. For small parameter shifting errors, the fault diagnosis accuracy is 90%. Take R6 for example. If R6 varies within the range of (0, 7kΩ)∪(13kΩ, ∞), it is diagnosed properly. When R6∈(7kΩ, 8kΩ)∪(12 kΩ, 13 kΩ), there are 5 percent of faults is not diagnosed. If its fault range is (8kΩ, 9kΩ)∪(11 kΩ, 12 kΩ), the fault diagnosis accuracy is decreased to 90%. Therefore, we can conclude that the proposed fault diagnosis method is not affected by tolerance problem. But the accuracy of small parameter shifting is susceptible to measurement error. The reason is that small parameter shifting incurs small differential voltage. Small differential voltage information is more likely covered by measurement errors. Therefore, the fault diagnosis accuracy is decreased. Even though, 90% fault diagnosis accuracy is acceptable.

Table 5 Fault diagnosis accuracy

| | faulty parameter range | | |
|---|---|---|---|
| | $(0.8R_0,0.9R_0)\cup(1.1R_0,1.2R_0)$ | $(0.7R_0,0.8R_0)\cup(1.2R_0, 1.3R_0)$ | $(0, 0.7R_0)\cup(1.3R_0, \infty)$ |
| R1 | 100% | 100% | 100% |
| R4 | 94% | 98% | 100% |
| R6 | 90% | 95% | 100% |
| R7 | 93% | 100% | 100% |
| R8 | 94% | 100% | 100% |
| R10 | 97% | 100% | 100% |

## Conclusions

The slope-based modeling method has solved the soft-fault diagnosis problem. However, the tolerance problem remains unsolved. The proposed phasor analysis and complex number decomposition based method can accurately model analog fault and is immune from tolerance problem. When combined with the Multi-class SVM technique, the proposed fault diagnosis method can accurately locate the fault component, even in the presence of a soft fault and tolerance. When a low magnitude parameter shifting happens, the component parameter shift just out of the tolerance limit for example, the measurement error might incur false diagnosis result. Even though, the accuracy is at least 90%. Additionally, the proposed method can readily be extended to multiple-fault situations. For example, to modeling and diagnosis double faults, all possible combinations of any two faults are listed. Same as single fault, for every pair of faults, the proposed simulation method is used to obtain fault voltage vector. Then the fault feature database is optimized and the Multi-class SVM technique can also be used to Multi-fault diagnosis.

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# Methods of Handling the Aliasing and Tolerance Problem for a New Unified Fault Modeling Technique in Analog-Circuit Fault Diagnosis

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**Keywords:** Analog fault diagnosis, fault modeling, tolerance, aliasing problem.

**Abstract.** Soft fault diagnosis and tolerance are two challenging problems in analog circuit fault diagnosis. This paper proposes approaches to solve these two problems. First, a complex field modeling method and its theoretical proof are presented. This fault modeling method is applicable to both hard (open or short) and soft (parametric) faults. It is also applicable to either linear or nonlinear analog circuits. Then, the parameter tolerance is taken into consideration. A frequency selection method is proposed to maximize the difference between the faults fault signature. Hence, the aliasing problem arise from tolerance can be mitigated. The effectiveness of the proposed approaches is verified by simulated results.

## Introduction

Among various fault diagnosis methods, one of the most widely used SBT methods is the fault dictionary method[1,2,3,4]. The fault dictionary technique is initially used in catastrophic faults diagnosis 0. Recently, it is extended to both hard-fault and soft-fault detection. In reference 0, a node-voltage sensitivity sequence dictionary method is established. Whether a fault is hard or soft, only one fault characteristic code is needed to detect any fault of a component. However, such a sequence is simples a qualitative signature and cannot explain the difference between any two signatures quantitatively, so it is unable to determine whether the real state of the circuits is within the tolerance range or under a fault state. Based on the ideas in Ref. 0, Ref. 0 developed a method for diagnosing soft faults of tolerance analog circuits and nonlinear circuits; while Ref. 0 constructed a new dictionary method based on a theorem referred to as "the conservation of node voltage sensitivity weight sequence". Wang and Yang 0 improved the method in Ref. 0, and then the fault dictionary method could theoretically achieve both single and multiple fault diagnosis, and handle tolerance. All the mentioned fault diagnosis methods and fault models can not properly solve the influence of tolerance on fault diagnosis.

A unified fault modeling method is proposed in this paper, and frequency selection method is proposed to solve the aliasing problem.

## Aliasing Problem of The Proposed Fault Model

It is proved0 that in a linear time-invariant circuit under test(CUT), the real and image parts of fault voltage must satisfy the following quadratic equation.

$$\Delta U_{or}^2+\Delta U_{oj}^2+\left(\frac{R_0}{X_0}n-m\right)\Delta U_{or}-\left(\frac{R_0}{X_0}m+n\right)\Delta U_{oj}=0 \tag{1}$$

where '$R_0$', '$X_0$', 'a' and 'b' are independent from the value of fault component $x$ and are uniquely determined by the fault free components in $N$ and the location of the fault element $x$; hence, formulation (1) always hold regardless of what kind of fault occurs to $x$, and can be used as the fault model. If $x$ is a dynamic element, the same conclusion is reached. Therefore, the equation (1) is a unified fault modeling method.

It is need to point out that equation (1) is also the function of frequency.

$$f_x\left(U_{or}, U_{oj}, \omega\right) = 0 \tag{2}$$

For lumped, linear, time-invariant circuits, the frequency response function is rational function in the frequency variable $\omega$ and the circuit elements $x_i$.

$$H(\omega) = \frac{N(\omega, x_1, x_2, \cdots x_m)}{D(\omega, x_1, x_2, \cdots x_m)} \tag{3}$$

Without loss of generality, suppose that the fault source is $x_i$ and all the other components kept constant, the frequency response function is the function of $x_i$

$$H_i(\omega) = F_i(\omega, x_i) \tag{4}$$

Because equation (1) is quadratic, the loci of any two different fault source on the complex plane might have intersections besides the fault free point, viz., for any two fault sources $x_i$ and $x_k$, there might be $x_{fi}$ and $x_{fk}$ such that the following equation established.

$$F_i\left(\omega_0, x_{fi}\right) = F_k\left(\omega_0, x_{fk}\right) \tag{5}$$

where $\omega_0$ is the operation frequency of CUT. It means that different faults may have the same output $\dot{U}_{ik}$ even if the fault sources are distinguishable.

Take Fig. 2 for example. R1 (signature curve ①) and C3 (signature curve ⑩) have different signature curves governed by equation(1). But besides the fault free point, either R1=3728 Ω or C3=73.5$n$ induce the same output $\dot{U}_f = -4.9 + 2.6\mathrm{j}$. Hence, these two specific parameter faults are undistinguishable at current frequency. It is referred to as aliasing problem in this paper. Methods are provided in the following section to solve such problem.

**Methods of Eliminating Aliasing and Tolerance Problem**

In analog circuit, a parameter of a circuit element may vary within a range around its nominal value, without treating it as a fault. This is termed "tolerance". As we know, due to the tolerance of analog components, the fault free voltage $\dot{U}_o$ in an actual circuit is definitely not equal to those obtained from simulation. That means the fault free point is shifted; hence, all signature curves are shifted and induce fault diagnosis failure. To mitigate these influences on fault diagnosis, this paper proposes three approaches:

[1] *To eliminate the influence on the fault free point*

When the circuit works steadily, voltage $\dot{U}'_0$ is measured. The fault free point is shifted by

$$\dot{U}_{shift} = \dot{U}'_0 - \dot{U}_0 \tag{6}$$

If a CUT fails and the corresponding output voltage is $\dot{U}_f$, the standardized fault voltage $\dot{U}_{sf}$ is

$$\dot{U}_{sf} = \dot{U}_f - \dot{U}_{shift} \tag{7}$$

[2] *To eliminate the aliasing problem*

A frequency selection method is proposed to select the optimum frequency to distinguish this kind of faults. In equation (5), there may be $\omega$ such that $F_i\left(\omega, x_{fi}\right) \neq F_k\left(\omega, x_{fk}\right)$. The idea is to select an optimum frequency $\omega_{ik}$ such that $\max_{\omega}\left\{abs\left[F_i\left(\omega_{ik}, x_{fi}\right) - F_k\left(\omega_{ik}, x_{fk}\right)\right]\right\}$ is achieved. At this frequency, faults xfi and xfk induce different outputs $\dot{U}_{fi}$ and $\dot{U}_{fk}$ respectively. At fault diagnosis phase, if the faulty output is around $\dot{U}_{ik}$, the frequency of the stimuli is adjusted to $\boldsymbol{\omega_{ik}}$, and the faulty output $\dot{U}_f$ is measured. If $\dot{U}_f$ is more close to $\dot{U}_{fi}$, viz. $abs(\dot{U}_f - \dot{U}_{fi}) < abs(\dot{U}_f - \dot{U}_{fk})$, the fault source is xi and vice versa.

**Process of The Proposed Fault Diagnosis Method**

[3] *Construction of fault dictionary*

Step 1) The CUT is stimulated at selected frequency $\omega_0$ and **fault dictionary figure** such as Fig. 2 is constructed.

Step 2) For any pair of faults (xi, $x_k$) that can be distinguished, except for the fault free scenario, finding the intersection points $\dot{U}_{ik}$ of the fault signature curves on complex plane. Output $\dot{U}_{ik}$ and corresponding fault values ($x_{fi}$, $x_{fk}$) that incur such intersection point are recorded.

For each pair of faults ($x_{fi}$, $x_{fk}$), the following frequency selection steps are executed.

Step 3.1) Except for that $x_i$=$x_{fi}$, all other components are fault free. By using the frequency sweeping function of PSPICE, $F_i(\omega, x_{fi})$ is obtained. $F_k(\omega, x_{fk})$ is achieved by using the same method.

Step 3.2) Frequency $\omega_{ik}$ that maximize $abs\left[F_i(\omega, x_{fi}) - F_k(\omega, x_{fk})\right]$ is calculated. $\omega_{ik}$, $\dot{U}_{fi}$ and $\dot{U}_{fk}$ obtained at frequency $\omega_{ik}$ are saved in a fault dictionary table for future fault diagnosis.

[4] *Fault diagnosis*

Step 1) The same stimuli, sinusoidal signal with frequency $\omega_0$, as that used in constructing the dictionary is applied to the CUT. The output $\dot{U}$ at selected test point is measured and saved.

Step 2) Standardized fault voltage $\dot{U}_{sf}$ is calculated

Step 3) If $\dot{U}_{sf}$ close to any intersection point $\dot{U}_{ik}$, go to step 5), else go to step 4).

Step 4) The stimuli frequency is adjusted to $\omega_{ik}$.Output voltage at this frequency is measured. Looking up the fault source in fault dictionary table.

Step 5) On fault dictionary figure, looking up the signature curve that close to $\dot{U}_{sf}$. The component corresponding to the signature curve is the fault source.

**Experimental Results**

The circuit is shown in Fig. 1. The excitation (input) signal is a 1kHz, 5V sinusoidal wave, and '***t***' is the test point.

• Constructing fault dictionary

By using the parameter sweeping function, all components' feature loci are simulated and shown in Fig. 2. The fault free voltage is $\dot{U}_o$=-1.84 + 0.98j. Simulated results show that the components in this CUT fall into several ambiguity groups, as shown in Table 1.

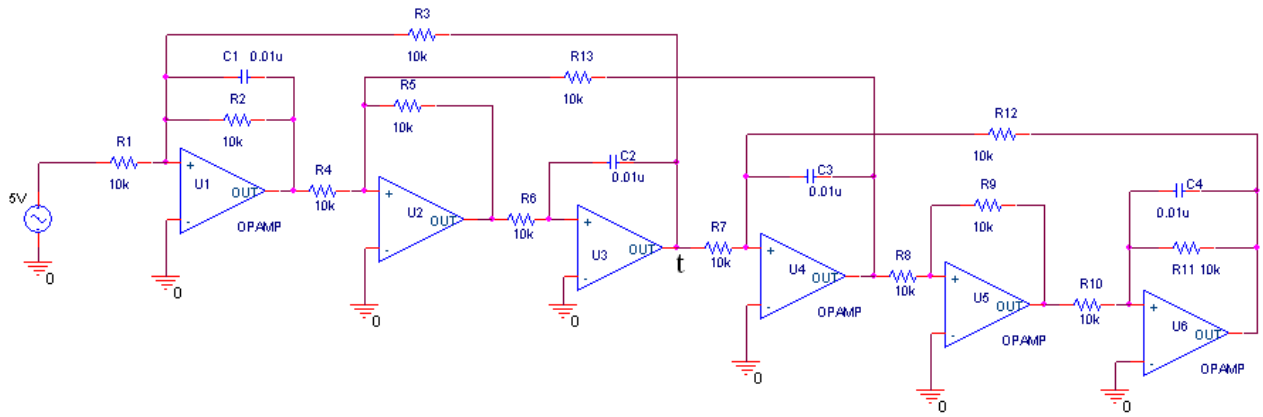


Fig. 1. Leapfrog filter

Table 1 Ambiguity Group of the CUT

| Ambiguity group | Fault component |
|---|---|
| ① | R1 |
| ② | R2 |
| ③ | R3 |
| ④ | R4 |
| ⑤ | R5,R6,C2 |
| ⑥ | R7, R13 |
| ⑦ | R8,R9,R10,R12 |
| ⑧ | R11 |
| ⑨ | C1 |
| ⑩ | C3 |
| ⑪ | C4 |

Each ambiguity group has a signature curve as shown in Fig. 2. This figure is saved as fault dictionary for future fault diagnosis. The aliasing problems, are solved as follows.

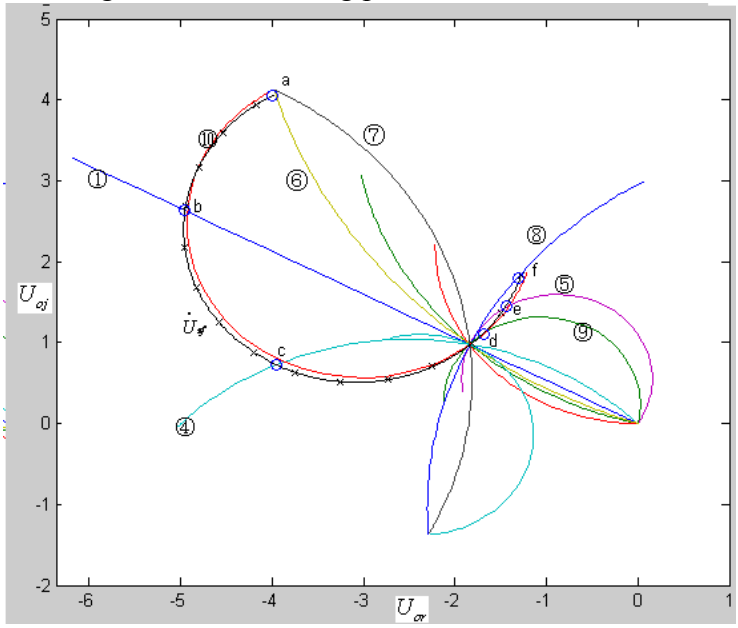


Fig. 2. Fault dictionary figure

Take R1 (signature curve ①) and C3 (signature curve ⑩) for example. R1=3728 Ω and all other components kept fault free. By using the AC sweeping function of Pspice, the output voltage $\dot{U}_{R1}(\omega)$ from 1 Hz through 10kHz are saved. C3=73.5n and all other components kept fault free, $\dot{U}_{C3}(\omega)$ is obtained. It can be calculated that $\max_{\omega}\left\{abs\left[\dot{U}_{R1}(\omega)-\dot{U}_{C3}(\omega)\right]\right\}$=11.32 is achieved at 2381Hz, and $\dot{U}_{R1=3728}$=-4.2+11.9j and $\dot{U}_{C3=73.5n}$=1.7 + 2.2j at this frequency.

In fault dictionary Table 2, $\dot{U}_f$, $\dot{U}_{R1=3728}$, $\dot{U}_{C3=73.5n}$ and $f$=2381Hz are recorded for future fault diagnosis. All other intersection points marked as black circles shown in Fig. 2 are handled by using the same method, and the results are shown in Table 2.

Table2 Fault Dictionary Table

| Intersection point $\dot{U}_{ik}$ at 1kHz | | Faults involved | | $\omega_{ik}$ | Output voltage at $f_{ik}$ | |
|---|---|---|---|---|---|---|
| | | $x_i$ | $x_k$ | $f_{ik}$:Hz | $\dot{U}_{fi}$ | $\dot{U}_{fk}$ |
| 1 | -4.93+2.62j | R1=3728 | C3=73.5 $n$ | 2381 | -4.20+11.86j | 1.72+2.22j |
| 2 | -1.40+0.62j | R2=6061 | C4=17.3 $n$ | 2319 | -1.55+2.96j | -2.25+6.00j |
| 3 | -2.21+2.30j | R3 open | R8=4339 | 2133 | 0.35+5.53j | -0.55+1.82j |
| 4 | -1.26+0.39j | R3=4007 | C4=21.4$n$ | 2339 | -2.04+1.03j | -1.31+6.65j |
| 5 | -3.87+0.76j | R4=2172 | C3=29.7 $n$ | 3636 | -3.66+11.14j | 0.99+0.55j |
| 6 | -2.80+1.03j | R4=5104 | C4 ≈ 0 | 2696 | -3.07+6.80j | 1.32+2.29j |
| 7 | -1.40+1.46j | R5=4908 | C3=4.3 $n$ | 3462 | 0.52+0.28j | -0.51+2.95j |
| 8 | -1.49+0.73j | R7=7235 | C4=15.3 $n$ | 2441 | -2.94+3.09j | -0.28+5.78j |
| 9 | -2.12+0.22j | R11=5265 | C1 ≈ 0 | 2531 | 0.85 + 4.21j | -2.96+1.88j |
| 10 | -1.68+1.11j | C1=12.9$n$ | C3=8.2$n$ | 2532 | -0.35+4.43j | -2.35+2.77j |
| 11 | -1.18+1.98j | R11=25.3k | C3 ≈ 0 | 2474 | -2.33+5.34j | 0.48+0.78j |

Fault diagnosis

Within the tolerance limit, $R_i \pm 5\%R_i$, $C_i \pm 10\%C_i$, all fault free components' parameter are randomly computer-generalized. The fault free voltage is $\dot{U}'_o$ = -1.75+1.02j.

As an example, all possible parameter shifting faults occur to C3 is considered, viz. C3=$\{0.001n \sim 9n\} \cup \{11n \sim 10^5 n\}$. The simulated faulty voltages are recorded and the standardized faulty voltage $\dot{U}_{sf}$ is calculated. Marked by '×', the faulty voltage $\dot{U}_{sf}$ is drawn in Fig. 2. It can be seen that far from the fault free and intersection points, signature curve of C3 (curve ⑩) is the sole curve that most close to $\dot{U}_{sf}$. On these conditions, fault source C3 can be diagnosed correctly.

When C3=30$n$, the simulated $\dot{U}_f$=-3.75+0.71j falls into circle 'c'. In the first column of Table 2, -3.87+0.76j shown in the 5th row is more close to $\dot{U}_f$ than others are. -3.87+0.76j is the common fault future of C3 and R4. To realize fault diagnosis, the corresponding frequency 3636Hz is applied to the CUT, and the output voltage 0.99+0.56j is obtained. From the 5th row of Table 2, it can be seen clearly that 0.99+0.56j is the fault signature of C3 at 3636Hz.

## Conclusion

The complex field fault modeling method introduced in this paper can handle both soft and hard fault diagnosis. Hence, it is a unified fault modeling method. This method needs only one test point, usually the output point, to diagnose fault component. Hence, it is especially applicable to CUT which has no inner accessible test points. Additionally, a frequency sensitivity method is proposed to solve the aliasing problem.

## Acknowledgements

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# Designing of New Intelligent Music Electro-acupuncture Apparatus

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**Keywords:** Music Electro-acupuncture Apparatus, electrical-stimulation adaptability, 1/f fluctuation, ARM

**Abstract.** The phenomenon of acupoint electrical-stimulation adaptability is common while traditional Pulse Electro-acupuncture (EA) Apparatus is used for treatment. To solve this problem, we designed an intelligent Music Electro-acupuncture (EA) Apparatus base on ARM9 and Linux. We analyzed power spectrum of music and put forward a possible screening technique for effective treatment music based on "1/f fluctuation" therapy. This system has excellent Qt user interface and touch screen. It is good for physical and psychological rehabilitation to listen to our music during treatment.

## Introduction

The waveform output from traditional Pulse EA Apparatus is repetitive pulse with fixed frequency and intensity, it is very easy to result in acupoint electrical-stimulation adaptability, which means that patients' needling sensation will be weakened and even disappeared with time, only by increasing the strength of electrical simulation can needling sensation be re-felt by patients. Acupoint electrical-stimulation adaptability has badly affected EA efficacy, hindered the development and promotion of EA. In this context, The Intelligent Music EA Apparatus avoided the effect of electrical-stimulation adaptability by applying Musical Electro-therapy and "1/f fluctuation" theory.

## Musical Electro-therapy

Musical Electro-therapy, using specific music signal acting on human body to treat diseases, is a new method which combines musical therapy with electrical therapy of traditional medicine. Experiments verify that Musical Electro-therapy has more advantages than traditional Pulse EA in some ways.

From the comparative observation of analgesic action of Music EA and Pulse EA on behavioristic and electro-neurophysiology, Hongsheng Dong [1] have confirmed that music EA had superiority on the analgesic action of rats, Musical Electro-therapy can overcome electrical-stimulation adaptability and played better acupoint function. From observation of the influence of the Music EA on the depression model rat hypothalamus and colonic mucosa β-endorphins (β-EP), Jinyan Teng [2] have concluded that Music EA can regulate the imbalance of brain-gut peptide in different regions, which provided practical approach to the clinical treatment of depression.

## "1/f fluctuation" theory

According to the corresponding relations between the Power Spectral Density (PSD) and Frequency (f), the fluctuation in the nature can be divided into three categories [3] as shown in Fig. 1. The first is white noise which is called $1/f^0$ fluctuation, its PSD parallels to the horizontal axis and has no link with f; The second is brown noise which is called $1/f^2$ fluctuation, its PSD is inversely proportional to $f^2$; The last noise, called 1/f fluctuation, is a disordered state locally while has certain relevance in the macro level, its PSD is inversely proportional to f.

If we use *x( t )* to represent 1/f fluctuation, the Fourier transform is

$$X_T(f) = \int_{-T}^{T} x(t)e^{-j2\pi ft}dt \ . \tag{1}$$

The PSD of *x( t )* is

$$S(f) = \lim_{T\to\infty} \frac{1}{2T} E\left[\left|X_T(f)\right|^2\right] . \tag{2}$$

The relationship [4] between PSD and f is

$$S(f) = A / \left|f\right|^{\lambda} . \tag{3}$$

In Eq.3, S (f) is PSD, A is a constant, f is the frequency and λ is the index of frequency. Take the logarithm of both ends of Eq.3, we will get

$$\lg S(f) = \lg A - \lambda \lg f . \tag{4}$$

In Eq.4, there is a linear relationship between lgS (f) and lg f, −λ is slope, when λ is 0,1 and 2, it is corresponding to $1/f^0$, 1/f and $1/f^2$ as shown in Fig.1.

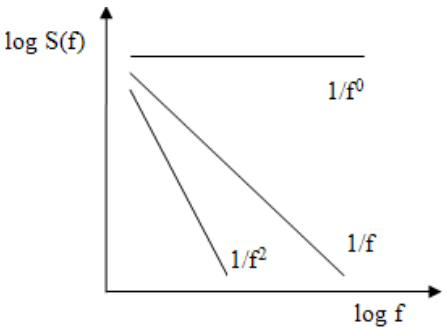


Fig.1 Spectral characteristic

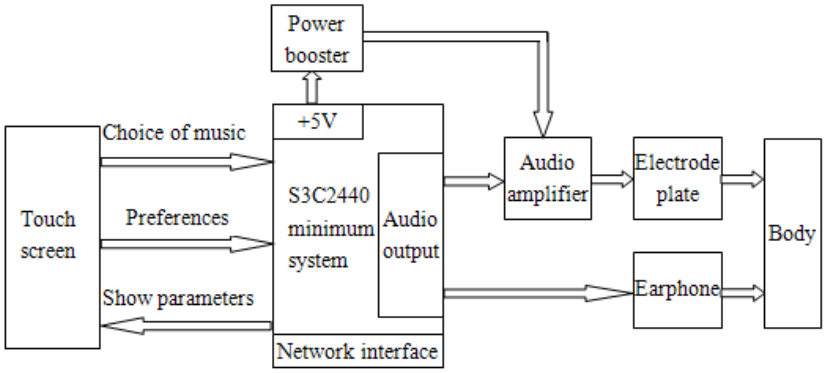


Fig.2 Hardware system block diagram

"1/f fluctuation" widely exists in the nature, such as refreshing breeze, the waves of the sea and the murmur stream; it also exists in the changing strength and rhythms of music. Studies [5] have shown that human being's heartbeat cycle in a comfortable state and α brainwaves' variation cycle are in accordance with "1/f fluctuation". "1/f fluctuation" of outside world can also inspire human being's α brainwaves to produce "1/f fluctuation" and make us comfortable. Based on above research, we can use "1/f fluctuation"theory to analyze music, screen out comfortable and harmonious music for Musical Electro-therapy.

## Hardware system design

The hardware system of Music EA Apparatus was composed of S3C2440 (ARM9 processor chip) minimum system, Power booster circuit, Audio amplifier circuit and Touch screen. As shown in Fig.2, the audio signal output from S3C2440 minimum system was ±500mV; one signal can be zoomed into ±7.5V to be applied to Musical Electro-therapy through Audio amplifier circuit, another signal provided patients of music appreciation through earphone; the +15V working voltage of Audio amplifier circuit was provided by Power booster circuit; by the graphical user interface, we can controll the therapeutic process. The network functions can be extended by Network interface and we

can build the doctor workstation to perform many other functions, such as information input and management of patients.

## Software system design

The software design of Music EA Apparatus was based on Qt, a cross-platform C++ graphical user interface library developed by the Norwegian TrollTech company. Qt has three notable features, one is that its cross-platform enable it can be run on Unix, Linux, Windows and many other platforms; two, Qt is based on C++ structure, thus enjoying all the advantages of object-oriented programming; besides, using underlying graphics functions from different platforms, Qt can simulate different styles of the platform, which is easy to use and with fast running speed. With Qt development interface and software flow chart shown in Fig.3, we realized functions such as open music files, display the list of songs, play music, select song playing order and the volume. Music EA Apparatus interface is shown in Fig.4.

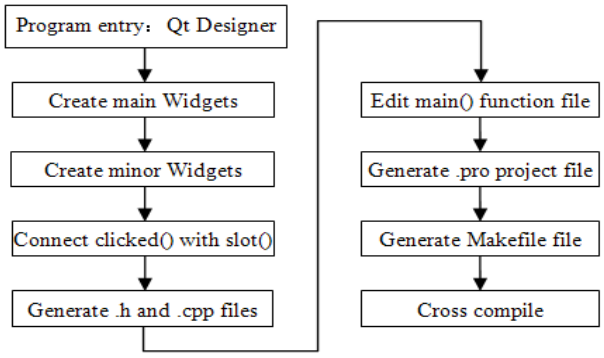


Fig.3 Software flow chart

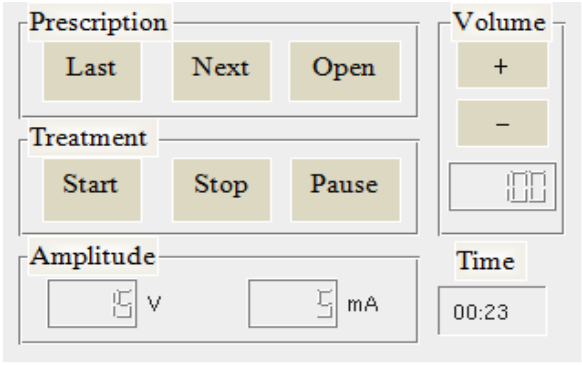


Fig.4 Music EA apparatus interface

## Test of electrical-stimulation adaptability

According to reference [6], in randomized controlled trial, we divided 20 volunteers into Pulse EA group and Music EA group equably. Then we used Visual Analogue Scale, VAS, to record the needling sensation values (0~50). At the beginning of test (0min), volunteers felt the needling sensation and set the value at the center of the VAS scale (5cm). Scale decrease meant the weakness of needling sensation and increase meant enhancement. The left boundary (0cm) stood for "no sense" and the right (10cm) was 2 times of the original value. During the test, volunteers were invited to point out the needling sensation at the 5, 10, 15, 20, 25, 30min of the test and the corresponding values were recorded. After that,we used SPSS17.0 to process recorded data and get a chart of needling sensation values(Table 1). variance approach was taken between groups to analyze repeated measurement data, and results are shown by mean ±standard deviation（$\bar{x} \pm s$）.

Table 1 Needling sensation changes of two groups（$\bar{x} \pm s$, mm , n=10）

| | Needling sensation values（mm） | | | | | | |
|---|---|---|---|---|---|---|---|
| Group | 0min | 5min | 10min | 15min | 20min | 25min | 30min |
| Pulse EA | 50.0 | 47.7±6.3 | 43.3±7.9 | 34.8±8.7 | 27.0±11.3 | 19.3±12.1 | 15.5±11.6 |
| Music EA | 50.0 | 51.2±1.6 | 53.8±3.1 | 53.3±2.4 | 53.7±1.6 | 53.8±1.7 | 53.3±2.7$^{\#}$ |

PS: compared to Pulse EA group, $^{\#}P$ <0.05

$P$ <0.05 meant difference of needling sensation values was statistically significant between Pulse EA group and Music EA group. In Table 1, values of pulse EA group decreased gradually with time, a clear decreasing trend arises after 10min, suggested the emergence of electrical-stimulation adaptability; on the contrary, values of music EA group shown trend of increase with time, the value

at 30min increased by 3.3 than that at 0min, suggested that music EA avoid electrical-stimulation adaptability.

**Test of "1/f fluctuation" law**

We used MATLAB to analyze "1/f fluctuation" law of music signals and get PSD trend of different music [7]. Take two songs,《My heart will go on》and《Rock On the New Long March》, for example. The former was a lingering melodious song whose PSD was shown in Fig.5; and the latter was a rock song whose PSD was shown in Fig.6. Compared the two figures we can know that PSD in Fig.5 was inversely proportional to f and lgS (f) was approximately linear with lgf, this coincided with 1/f fluctuation law. But in Fig.6, the relationship between PSD and f was complicated, and it does not meet 1/f fluctuation law. In this way, we picked out the music whose PSD had 1/f fluctuation characteristic from those had not, and took them as prescription of Musical EA apparatus.

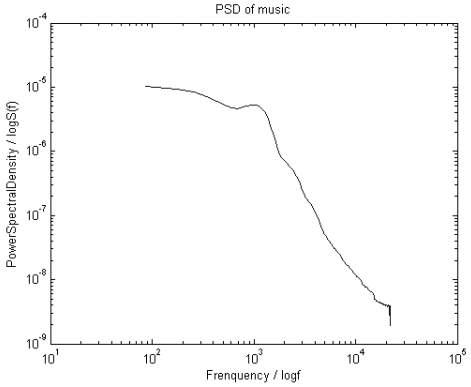


Fig.5 PSD of 《My heart will go on》

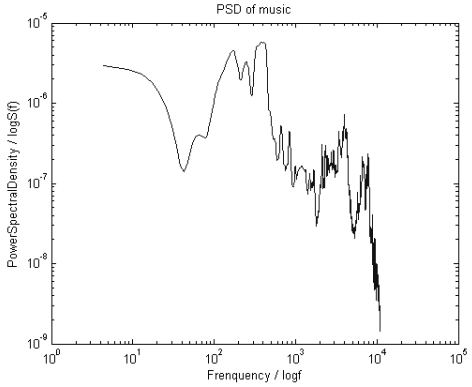


Fig.6 PSD of 《Rock On the New Long March》

**Conclusions**

In this paper, Embedded ARM technology was used to devise an intelligent Music EA Acupuncture. Experiment verified that it could avoid the effect of electrical-stimulation adaptability. We analyzed music power spectrum by MATLAB, and put forward a possible screening technique for effective treatment music. We find that it's theoretical reasonable for music with character of "1/f fluctuation" to be a treatment. Compared with Pulse EA Acupuncture, intelligent Music EA Acupuncture has high efficient Linux systems and Qt graphical user interface which is easy to operate. It has great practical significance as medical equipment for clinical study and home health care.

**Acknowledgements**

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# Research of Low Power Design Strategy Based on IEEE 1801 Unified Power Format

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**Keywords:** IEEE 1801, UPF, low power, power consumption

**Abstract.** Power consumption is becoming an increasingly important aspect of circuit design. High power consumption can lead to high machine temperature, short battery life which makes laptop electronics difficult to be widely used. IEEE 1801 Unified Power Format (UPF) is designed to express power intent for electronic systems and components .This paper first introduces the power principles, puts forward the approaches to reduce power consumption according to UPF, and then demonstrates the Synopsys design flow based on UPF, finally gives the power report and makes a conclusion.

## Introduction

In recent years, the device densities and clock frequencies have been higher and higher, at the same time, the supply voltages and transistor threshold voltages have been lowered in CMOS devices, so power consumption has been dramatically increased. Increased power consumption can lead to a series of headache problems such as high machine temperature which makes users uncomfortable and requires expensive cooling systems, low battery life which restrict the widely use of laptop electronics. For millions of computers, servers, and other electronic devices used on a large scale, even a little rise of power consumption can cause enormous electrical energy waste. At the same time, even a small reduction in power consumption can result in large aggregate cost savings and can provide significant benefits to the environment as well[1].

The Unified Power Format (UPF) is a standard set of Tcl-like commands used to specify the low-power design intent for electronic systems. The official Unified Power Format, version 1.0,was approved in February 2007 by Accellera. Accellera is an electronics industry organization focused on creating electronic design automation standards that can be used throughout the industry. Accellera transferred the UPF copyright to the IEEE P1801 Working Group for further expansion and refinement of the power specification standards and for formal approval as an IEEE standard. IEEE 1801™-2013 ", the newest revised version, was announced at 30 May 2013 [2].

## 1. The types of power

There are two types power that we must consider during chip operation, dynamic and static power.

### 1.1. Dynamic power

Dynamic power is the energy consumed during logic transitions on nets, consisting of two components, switching power and internal power.

Switching power results from the charging and discharging of the external capacitive load on the output of a cell. Switching power consumption depends on the clock frequency (possible transitions per second) and the switching activity (presence or absence of transitions actually occurring on the net in successive clock cycles).

Internal power results from the short-circuit current that flows through the PMOS-NMOS stack during a transition. When the input signal is at an intermediate voltage level, the PMOS and NMOS transistors can be conducting both. This condition results in a nearly short-circuit conductive path

from VSS to ground. Lower threshold voltages and slower transitions result in more internal power consumption.

### 1.2. Static power

Static power is also called leakage power which is caused by leakage current including reverse-bias p-n junction diode leakage, subthreshold leakage, and gate leakage. Leakage power is becoming increasingly significant with shrinking device geometries and reduced threshold voltages. Leakage currents occur whenever power is applied to the transistor, irrespective of the clock speed or switching activity. Leakage cannot be reduced by slowing or stopping the clock.

However, it can be reduced or eliminated by lowering the supply voltage or by switching off the power to the transistors entirely.

## 2. Low power design strategy

There are many kinds of ways to reduce power, such as clock gating, dynamic voltage, and frequency scaling etc. And most of these strategies can be implemented using UPF commands.

### 2.1. Clock gating and power switching

Clock gating has been used widely and successfully for a long time. In some circumstance registers need to maintain the same logic values over many clock cycles. Reloading the registers with the same value on each clock cycle causes power waste. If the clock is gated, the power will be reduced. According to the design, clock gating can be inserted intently during RTL design. Synthesis tool for example design compiler (DC) can also find low-throughput data paths and automatically done this work. This kind of work can be checked from the command log file.

Power switching is different from clock gating because parts of the chip are shut down completely during periods of inactivity by cutting the supply voltage which is called power down mode. Before they are in use, they must be “wake up”. In power down mode, there is no leakage and switching power, which can dramatically reduce power consumption. The implementation of power switching needs the help of a power controller, a power-switching network, isolation cells, and retention registers. A power controller is a logic block that determines when to power down and power up a specific block. The network connects the power to or disconnected the power from the logic gates in the block. Isolation cells are used to connect power on module and power down module. When both modules are on, they like wires. When one is off, they can provide a known, constant logic value to an always-on block. Before power down, the value of registers should be saved and restored after power on by retention register. The relevant commands of UPF are create_power_switch, map_power_switch, set_isolation, and set_retention etc.

### 2.2. Dealing with voltage

Supply voltage reduction can reduce power effectively. According to the formula Power = IV = V2/R, A 50 percent reduction in the supply voltage results in a 75 percent reduction in power. But lower voltage can cause low speed and some other problems, such as, noise immunity, crowbar currents, and sub-threshold leakage. Of course, different parts in a chip might have different speed. So multivoltage can be implemented to save power. Even the voltage can be changed dynamically according the operating status. So is the clock’s frequency. The relevant commands of UPF are create_power_domain, create_supply_net, create_supply_port, set_domain_supply_net, and so on.

### 2.3. Using Multiple-Vt Library Cells

Some CMOS technologies support the fabrication of transistors with different threshold. The cells have the same logic function but different transistor threshold. Low-Vt leads to higher speed, and higher sub-threshold leakage current. High-Vt leads to low leakage current, but less speed. Synthesis’ tool can decide which cell to use. When timming is critical, low-Vt cells are used. When timing is loose, High-Vt cells are chosen. High-Vt transistors are used as power switches and retention register because they minimize leakage and their switching speed is not critical.

## 3. The Synopsys low power flow

The Synopsys low-power flow is shown in Figure1. First Design Compiler reads in the RTL and UPF1 files, and synthesizes a gate-level net list and a UPF2 file. The DC commands are Load_upf and save_upf. Then IC Compiler reads in the gate-level net list and the UPF2 file, after physical implementation produces a modified gate-level net list, a complete power and ground (PG) netlist, and an updated UPF file. VCS and MVSIM can be used for functional verification of the multivoltage design. MVRC checks for adherence to multivoltage rules and reports any problems related to power. PrimeRail performs voltage drop and electro migration analysis for gate-level and transistor-level designs. PrimeTime does timing analysis with UPF information.

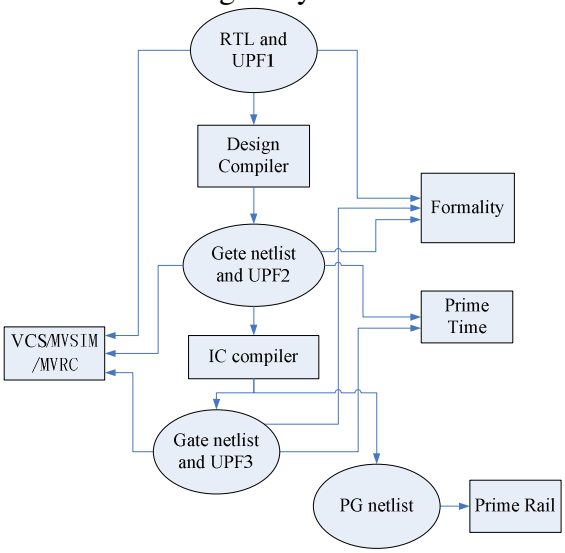


Figure1 Synopsys low-power flow

## 4. Report analysis

TSMC is the world's largest dedicated semiconductor foundry. It supplies 180nm CE018FG ULL (ultra low leakage) technology library to support ultra low power design. Synthesis base on UPF using ULL (ultra low leakage) technology library and normal flow using base technology library are done respectively, and two different power reports are got. The contrast between them is shown in table1.

Table1 Contrasts between two design flows

| category | | ULL flow | | Normal flow | |
|---|---|---|---|---|---|
| total dynamic power | cell internal power | 4.4750 mW | 8.1424 mW | 6.5583 mW | 12.2461 mW |
| | net switching power | 3.6673 mW | | 5.6879 mW | |
| static power | Cell leakage power | 1.9220 uW | | 13.2836 uW | |

From the data of table, both the static and dynamic power is reduced. DC is not expert power analyzer. Comprehensive power analysis should be performed by Primetime PX after physical implementation.

## 5. Conclusions

With the improvement of science, plenty of electric devices consume enormous energy. Energy consumption causes the worse environment on the earth. Reduction power consumption becomes extremely urgent. Low power strategy base on IEEE 1801 Unified Power Format can reduce power consumption of chips dramatically. With the wide application of this technology, the problems will be solved finally.

**Acknowledgements**

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# The Key Technology of Designing the Universal Programmer for Freescale HCS12 Serial MCUs

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**Keywords:** Programmer, Freescale HCS12, BDM, high-speed downloading, Erase, Write

**Abstract.** For implementing on-line programming of Freescale HCS12 series MCU, designing a common downloading programmer which functions include chip selection, erase and write operations. Designing a database where Freescale HCS12 MCU Flash difference parameter values placed, so achieving HCS12 MCU family online programming versatility. Erase and write machine codes are provided in the RAM area of Flash memory, these codes will be run at high voltage, these codes are relocated from Flash to RAM area for improving flash operation stability during the high voltage. According to BDM communication theory, we have developed a separate BDM serial communication program, the target device only receives the user code from the programmer, programmer does not need send opcode and the address information, not waiting for a command, so, increasing the erase and write speed. the programmer has the versatility and easily using.

## Introduction

Now, the CodeWarrior is the integrated development environment(ie,.IDE) for the Freescale HCS12 serial MCUs and is largely impacting on the market, it is functional, stable performance, but expensive, so it is not suitable to teaching and development for the embedded area. The universal programmer for the Freescale S12 MCU in this paper is the BDM debuger tool which supporting the Freescale MC9S12 series, MC9S12X MCU, it could implement the writing and erasing operations for all 16-bit Freescale MCUs. through studying the common and difference features of the Freescale HCS12 series MCUs, the key technology of the versatility and high-speed downloading of the programmer are given.

## Overview

The universal programmer for Freescale S12 serial MCUs is the BDM debugging tool for the 16-bit MCU of Freescale, the core chip of the programmer is MC68HC908JB8[1], communicates with the target board by the BDM way[2], and communicates with the PC by the USB interface, and the USB interface can provide working power of the target board, the system block diagram is shown in Fig.1 to implement the BDM way communication, the programmer also needs the BDM driver module.

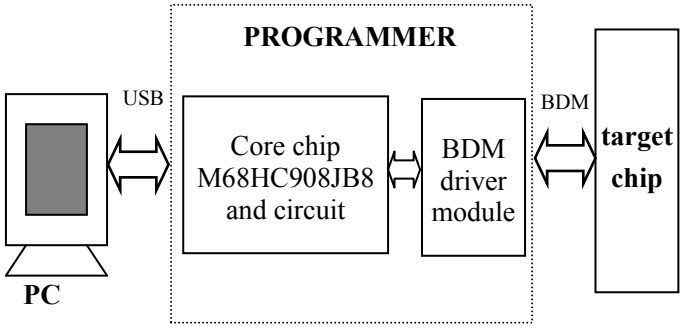


Fig. 1. Programmer system diagram

## System design

The design of system software including: communication program interface design, PC programming, MCU flash programming. When the flash erasing and writing operations of the target chip is runing, Firstly, PC needs to get the user instructions, and then call the corresponding erasing and writing codes of MCU, and these codes are writen to the Specified RAM area of the target chip. Finally, PC program run the command of turnnig to erasing-writing address in the RAM area, and execute the erasing-writing codes. When the PC communicates with the MCU, communications program need to call the appropriate dynamic-link library files:TBDML.DLL, which provided by Freescale company [3].

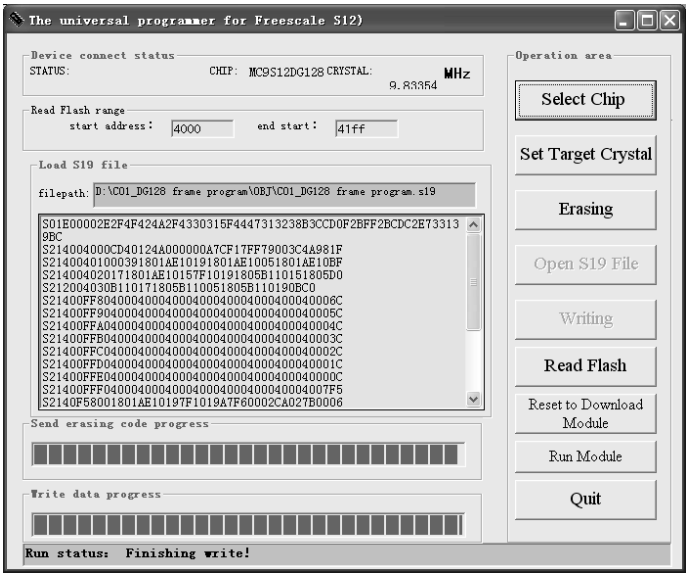


Fig 2. Programmer PC operation screen

## PC software design

1) main module

The view chart of PC program running[4]as shown in Fig.2, the module's main flow chart is shown in Fig.3.

Programmer communication process is as follows:

① PC sends the command of entering the BDM, then the target chip is into the BDM mode;

② PC sends the command of completely erase, the target chip Flash is erased, and checked, then returning checkedcode;

③ PC sends the commands of downloading the write subprogram code into the target chip memory, the function of write subprogram is that the user target codes stored in the chip memory are written to ROM Flash;

④ PC analysis S19 files, extracting the target code being sent, combining 512 bytes into one page, sending to the target chip memory via paging, and then running the writing subprogram stored in the RAM area, the user object codes are written to ROM Flash area;

⑤ PC could detect whether or not to send the next page, and receive a check code to determine correctness of the sending data.

After starting the program, at first, detecting device connection, if unconnected,returning error message ,and prohibiting the following erasing and writing operations.

If the initialization process is completed and the chip successfully enter the BDM mode ,then,the system is waiting for the user operating instructions,which is as shown in Fig.3. After completing the necessary operations, the user can execute quit to turn off the device and exit the main program.

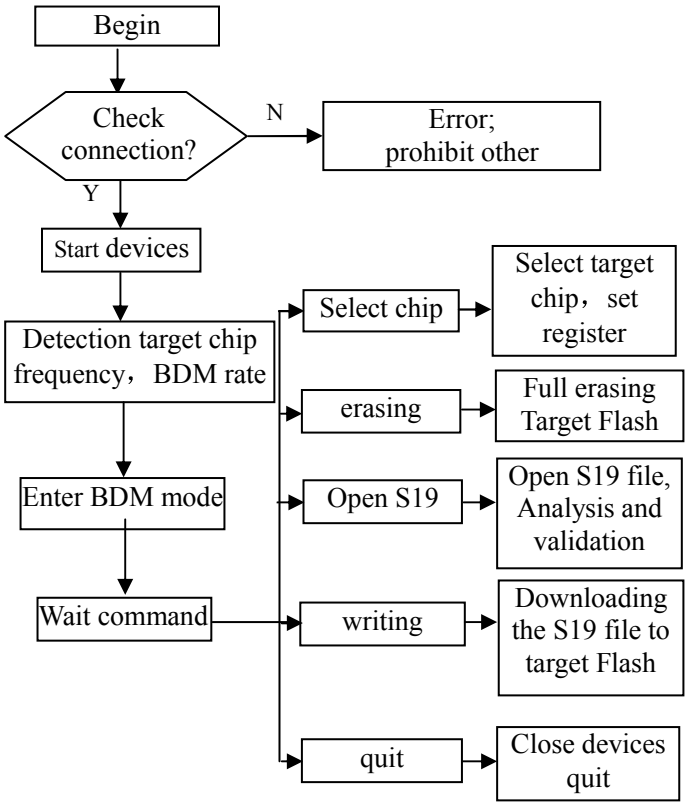


Fig.3. Main program flow chart

Programmer universal design

It is important for the key technology of universal design to deal with the FLASH parameters of HCS12 series MCU[5]. It is necessary to in-depth understanding, comparing and summarizing the FLASH parameters of different chips before you will design the program downloading module.When the different FLASH parameters of the different chips are obtained, they should be put into the database, so,when downloading program, the related chip parameters could be read from the database.Now, PC software can read the parameter values from the configuration file and database according to the selected MCU type these parameter values are necessary to design the erasing-writing program of the target chip The following table shows some important parameters of the several chips of the HCS12 series MCUs, these parameters value may be different for different MCU.When the user data of one page is written to the RAM area, the start address of user data stored in RAM area will be different, so it is variable parameters, and can be read from the database.

Table 1 Some MCU parameter

| chip name | user data start address | flag bit start address | writing file path | erasing file path |
|---|---|---|---|---|
| MC9S12DB128 | 0x1A00 | 0x19FE | .\DB128Write | .\DB128Erase |
| MC9S12DG128 | 0x1800 | 0x16FE | .\DG128Write | .\DG128Erase |
| MC9S12DJ128 | 0x1800 | 0x16FE | .\DJ128Write | .\DJ128Erase |
| MC9S12NE64 | 0x3000 | 0x2FFE | .\NE64Write | .\NE64Erase |
| MC9S12UF32 | 0x1800 | 0x16FE | .\UF32Write | .\UF32Erase |
| MC9S12xDP512 | 0x2800 | 0x27FE | .\S12XWrite | .\S12XErase |

Flag bit start address: the parameter is an address of RAM area,the flag sign of the success or error of erasing-writing opreration is stored here,two bytes.After one page user data is writen completely,

PC must read a word from this address to judge the success or failure of Flash writing operation, only success, the next page user data could be writen.

Writing and erasing file path: because the FLASH parameters and space of each MCU are different, their erasing and writing program code are different, therefore, PC need to call writing program code files (* Write.s19) or erasing program code files (* Erase.s19) according to the currently selected chip name and operation type.PC calls the * Write.s19 file when the writing operation is executed.the erasing operation is too.the two file path could be read from the database.

b) Programmer high-speed downloading design

By optimizing the communication subfunction code, the time spending on sending data from the JB8 chip memory to the target chip memory can be greatly reduced, but when executing BDM command, in addition to sending 2 bytes of user data, but also sending some extral bytes, and the completion of the command will require a longer delay.Because the single-pin BDM serial communication is used, you can design the function which simulating BDM serial communication,the target MCU only receives user object code from the programmer,so improving communication speed.

Furthermore, the PTB.0 pin of JB8 connect with PTA.0 pin of the target MCU, BKGD pin is unaffected during the data communication. Communication process is as follows:

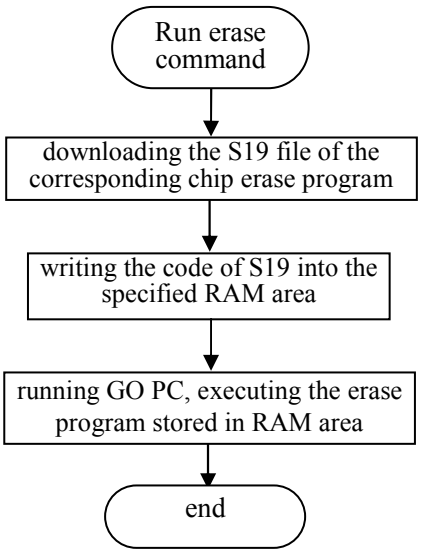


Fig.4. Erase program flow chart

① in accordance with the sequence that programmer sends a bit data, the function sending byte via PTB.0 pin are designed;

② in according to the process of receiving a bit data of the target chip, the function receiving byte via PTA.0 pin,and then designing target chip receive function;

③ the target chip receive function are compiled into object code, then the code is sent to the target MCU RAM area by executing BDM command.

④ executing the target chip receive function, the bytes received will be written to the specified ROM area of the target MCU.

Since the target chip receive function is own definition, the programmer need not to send opcode and address information, and need not wait for command completion. The code size of the target chip receive function less than 50 bytes, the time speding on sending them is very short.Thus, if the programmer sends the100KB data to the target MCU RAM,the time spent is calculated as follows:

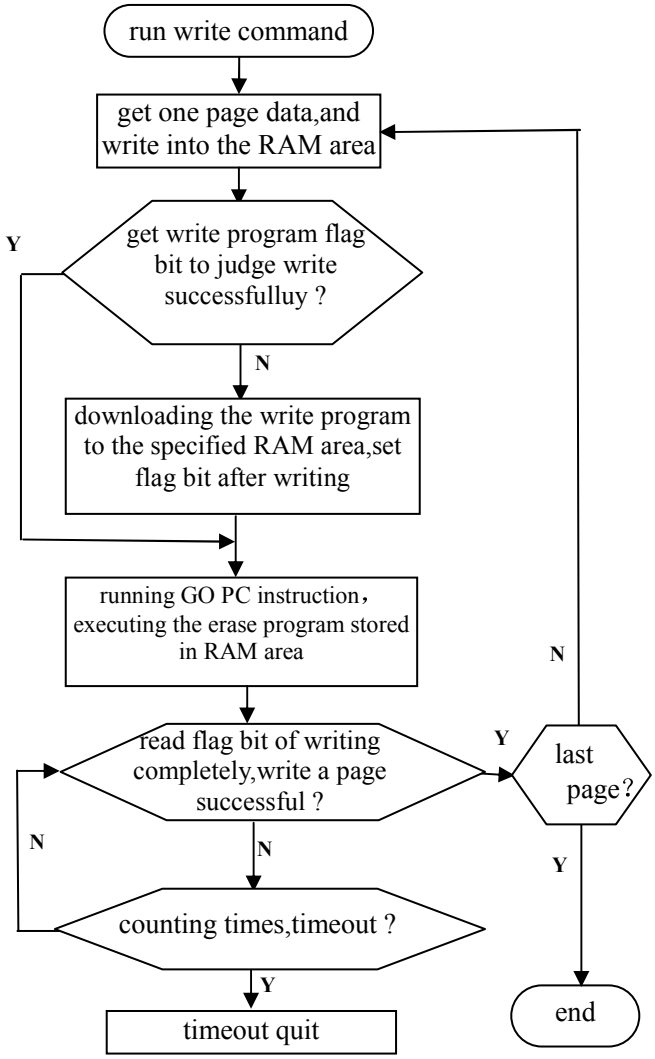


Fig.5. Write operation flow chart

(100 × 1024) bytes × 809 cycles ÷ (24 × 106) = 3.45 s

After using the function, the downloading speed of the programmer is increased by 8 times.

2) Erase module

The flow chart of erase function is shown in Fig.4. After obtaining the erase command, at first, the main module loads erase file of the corresponding chip, then,writing the S19 code of erase function to the target MCU RAM area, and executing GO PC instruction,so the target MCU turned to the address where the erase function code stored ,and run the function,and the corresponding Flash area is erased[6].

3) Open and analysis S19 module

Executing the operation, firstly ,the main module read the open S19 file by line ,and save the data to a string array, at the same time,verify the checksum,the array element contains the line data of S19 file.Then the data are recombinated in pages ,and saved to a new string array, but the space of previous array should been released.

4) Write module

The flow chart of write function is shown in Fig.5. After obtaining the write command, t firstly ,the main module get a page data,and writing it to the corresponding RAM area, then judge the success or failure of write operation, if it is failure, then writing again. then executing GO PC instruction,so the target MCU turned to the address where the write function code stored ,and run the function,and

waiting for the completion of one page data writed,if the wait time is too long, and quit the operaton, otherwise,could write the next page,the write operation is all completion until the last page.

***MCU flash programming***

MCU erasing-writing funciton is to erase and write the target chip Flash area [7]. Flash could not be read during executing erase and write process of Flash, , so the erase and write funtion code shuld to be placed in Flash RAM, that is, before erasing or writing Flash, the PC software should take the erase or write executable code into RAM, and run them in RAM.

The step of Flash erase and write operation is as follows.

① clearing the ACCERR and PVIOL, which is the error flag bit of the FSTAT that is the Flash status register;

② writing the b1 and b0 bit of FCNFG that is the Flash configuration register, for example, the the two bit value of MC9S12DP256 determine to use which 64KB of the 256KB Flash;

③ writing PPAGE register;

④ Checking the last Flash operation command is finished or not, if not, couldn't write a new command;

⑤ writing the data word to the appropriate address, the address must be an even address;

⑥ writing the command word to the FCMD register, the 0x41 is the command word of the overall erase, the 0x20 is the command word of the single-byte write;

⑦ writing 1 for clearing to CBEIF bit of FSTAT that is the Flash Status Register.then the CCIF bit in the status register will be set, which indicating a successful clearing operation.

## Conclusion

This paper design a universal programmer,which can program a serie MCUs of Freescale S12.The programmer Use MC68HC908JB8 as the core chip,and communicating with the high-end by USB,and communicating with the MCU by BDM. Not only the MC68HC908JB8 MCU selected is cost-effective, but also the operation of its own USB module is convenient and reliable. The programmer is reliable and low cost, the user can design the programmer of other series MCU by modeling on this programmer, but the MCU must support the BDM standard.

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# A Design of High Performance CMOS Folded Cascode Operational Amplifier

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**Keywords:** high performance; folded cascode; amplifie

**Abstract.** This paper describes a kind of folded cascode amplifier, which not only has high gain, large output swing characteristics, and its outputs can be self-compensation, it has a strong suppression capability with voltage noise. Based on a 0.5μm CMOS process uses two operational amplifiers. Through software emulation corrected the error which was caused by theoretical calculation. Has good performance in gain, noise, swing, phase margin, common mode rejection ratio and other parameters.

## Introduction

With the rapid development of very large scale integrated, analog integrated circuits have been developed by leaps and bounds as well. Amplifiers, filters, feedback circuits, reference circuits, switched capacitor circuits and many other circuits could be constituted by analog integrated circuits though its different forms. It was applied in radar, aerospace, surveying, storage and many other areas. So the requirements of accuracy, speed and efficiency is increasing. With the improvement of the level of technology, a new epoch is waiting for analog integrated circuits. Operational amplifiers as one of the most common units of analog integrated circuits. Depend on its large bandwidth, large swings and high speed, folded cascode amplifier get more attention by people [1]. The paper design a kind amplifier circuit of folded cascade for integrated CMOS, realization of high gain and voltage noise suppression by two cascaded op-amp, and be verified through software emulation.

## Principle And Structure of Circuit

Folded cascode amplifier can overcome the small output voltage swing disadvantages of telescopic cascode amplifier. Folded cascode amplifier is constituted by common source tube and common gate tube parallel transverse [2]. The basic design idea of folded cascode amplifier is transform input voltage to current, then as the input terminal of common source tube. The basic structure of folded cascode amplifier as is shown in picture 1.

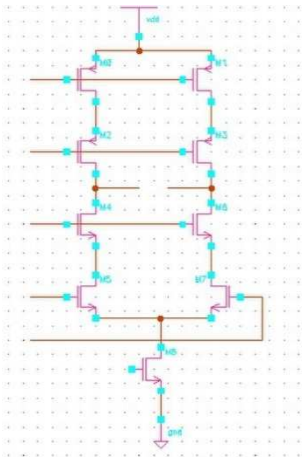

Figure 1 The basic structure of folded cascode amplifier

The folded cascode amplifier can be divided into two parts, the first portion of the circuit provides a low noise input stage. The noise from the back of the circuit will be amplified by the first stage, we have to reduce the noise in the first stage circuit. So we will choice differential input amplifier circuit structure. Meanwhile adopts cascode circuit structure in order to improve the circuit gain and output swing. The second part is an inverter structure, swing and gain will be controlled within a desired range. The overall structure of the operational amplifier is shown in Figure 2.

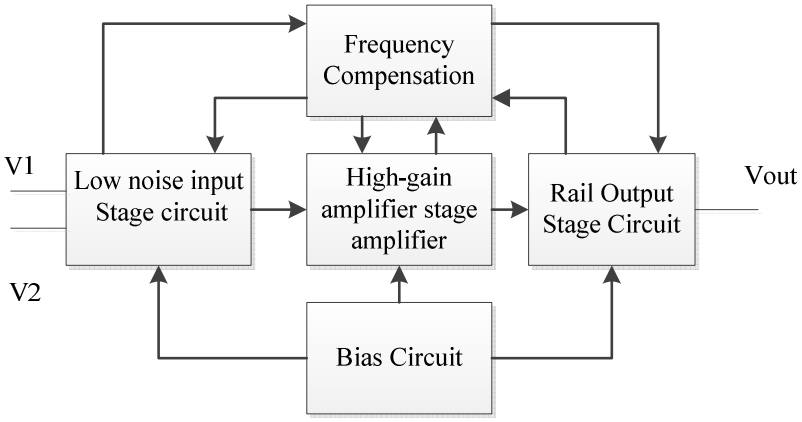


Figure 2 The overall structure of the amplifier

## Circuit Design

**The Overall Design.** Folded cascode amplifier design is shown in Figure 3. $M_0$, $M_1$ provides a paranoid current for amplifier circuit. $M_2$, $M_3$ are NMOS input common-source amplifier tubes, and make the input common-mode voltage range greater. $M_4$ provides tail current for differential amplifier. M5 and $M_6$ are PMOS cascode amplifier tubes. $M_7$, $M_8$, $M_9$, $M_{10}$ is the low-voltage NMOS wide-swing cascode current mirror. They are used as the active load of the differential amplifier, and converted the differential current to a single-ended output voltage. $M_{15}$ and $M_{17}$ constitute the structure of the output stage. Wherein the $M_{15}$ selected PMOS as input pipe and $M_{17}$ was used as a current load.

**DC Gain.** DC gain is one of the most important indicators of amplifier design, affects the precision of operational amplifier system [3]. With open-loop gain increases, may reduce voltage swing. Generally, we take to reduce the paranoid current approach to improve open-loop gain [4]. The amplifier gain is expressed as:

$$AV=Gm*Rout \tag{1}$$

Gm is the trans conductance of the input differential stage, Rout is the output resistance. For the folded cascode amplifier we know that, the output Resistance of cascode current mirror parallel the output Resistance of cascode amplifier is the small signal output resistance:

$$R_{out} \approx [(g_{m6} + g_{mb6})(r_{ds3} \| r_{ds1}) r_{ds6}] \| [(g_{m8} + g_{mb8}) r_{d8} r_{d10}] \tag{2}$$

$g_{m6}$, $g_{m8}$ are the transconductance value of $M_6$, $M_8$. $g_{mb6}$, $g_{mb8}$ are the transconductance value which caused by bulk effect. $r_{ds8}$, $r_{ds10}$ are the internal resistance value of $M_8$, $M_{10}$. $rds_1$, $r_{ds3}$ are the output resistance value of $M_1$, $M_3$ when operating in the saturation region.

If we ignore the bulk effect, the single-ended small-signal voltage gain is:

$$A_{vd} = \left| \frac{V_{out}}{V_{id}} \right| = g_{m2,3} \{ [g_{m6} r_{ds6} (r_{ds3} \| r_{ds1})] \| g_{m8} r_{ds8} r_{ds10} \} \tag{3}$$

$g_{m2}$, $g_{m3}$, $g_{m6}$, $g_{m8}$ are the transconductance value of $M_2$, $M_3$, $M_6$, $M_8$. $r_{ds1}$, $r_{ds3}$, $r_{ds6}$, $r_{ds10}$ are the output resistance value of $M_1$, $M_3$, $M_6$, $M_{10}$ when operating in the saturation region.

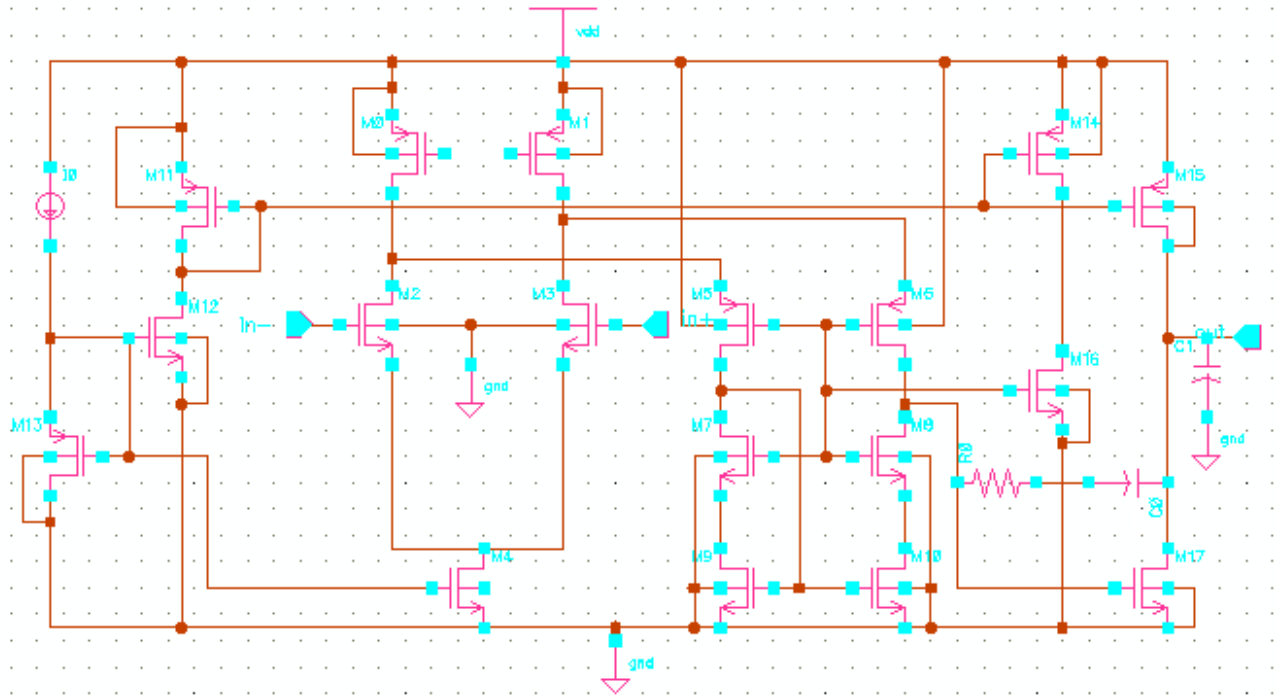


Figure 3 The amplifier circuit diagrams of folded cascode

**Output Swing.** Operational amplifier output swing to represent the greatest undistorted voltage at the output range. It is related to output stage circuit structure, size and paranoid current. We managed to improve the output voltage swing by increasing the width to length ratio of MOS, but note that this will also increase the parasitic capacitance, and make the frequency characteristic of the system drops.

To make the output swing is large enough, we will let the input common source tube and the output a total of cascade tubes respectively the NMOS and PMOS, then the input and output shorted to play a role in increasing the swing. The same time as the permissible range of input vcm increases, select the input vcm value becomes much easier [5].

**Common Mode Rejected Ratio.** The ratio of difference-mode voltage gain and common mode voltage gain is common mode rejected ratio, it represents the ability of which the op amp suppress common mode voltage [6]. For the ideal operational amplifier, $A_{vc} = 0$, so the CMSS should be infinite. However, the actual circuit will decrease due process limitations. It expression is:

$$CMSS = | Avd/Avc | \quad (4)$$

Avd is difference-mode voltage gain, Avc is common mode voltage gain.

***Phase margin.*** Pm size determines the stability and transient response of the entire system, generally for the integrated circuit amplifier designs [7], 60° PM best meet the design requirements.

***Slewing Rate.*** SR of a system is determined by tail current differential amplifier and phase compensation capacitor, although the increase in tail current can be increase SR, but also make the system power consumption increases, so we should adjust the appropriate tail current and phase compensation value, and make the circuit reach the design standards what we want. When operational amplifiers processing high speed and large signal swing, we need to increase the value of the SR to prevent the output signal distortion [8]. Slew rate expressions are as follows:

$$SR=I/Cc \tag{5}$$

I is tail current differential amplifier, $C_c$ is Phase compensation capacitor.

As folded cascode amplifier has high output impedance characteristics, the output capacitance is also usually relatively large. Its main poles are generally located in the output of the circuit affected by output resistance and load capacitance. We all know that load capacitance has a phase compensation effect, increasing the load capacitance can make larger phase margin. If the load capacitance is too small, it will lead to the main poles and other poles cannot be separated, the phase margin may not meet the requirements. If the load capacitance is too large it will affect the bandwidth and speed of the system, so we need to choose an appropriate compensation capacitor to meet the design requirements [9].

**The Results of Simulation Analysis**

To test the correctness of folded cascode amplifier design, through analysis and calculation. The size of each MOS transistor and related parameters were designed which based 0.5 μm CMOS process. Applying simulation software circuit to carry out multiple simulations, making the corresponding adjustment for the ratio of width and length of every MOS tube. In the end get the output waveform of the circuit.

Figure 4 is open loop gain of the op-amp and the curve of phase margin. Through simulation we can see that the open-loop gain of the amplifier reaches 92dB, meets the design requirements. And the phase margin of the amplifier is 76°, with good stability. However, as previously mentioned, Its Time response speed is relatively slow.

Figure 5 is input noise graph of the op-amp, in this paper, equivalent voltage of input noise is $9.256\,\mathrm{nV}/\sqrt{Hz}$, as to the mill volt level change of the input signal, its influence is very small, which Shows the differential structure can efficiently reduce the noise effect to the circuit.

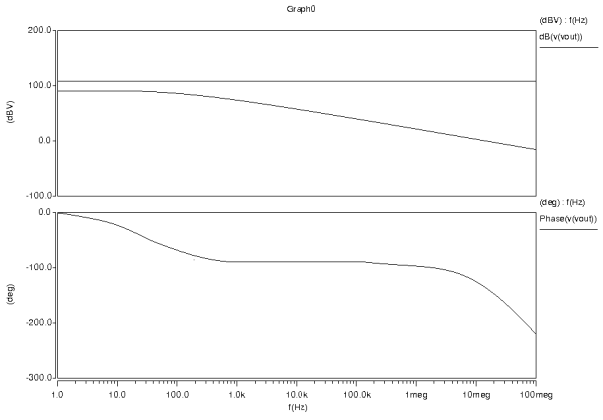


Figure 4 Op amp's open-loop gain and phase margin

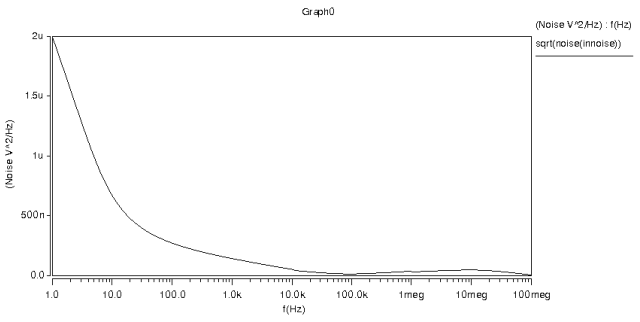


Figure 5 Characteristic curve of input noise

Figure 6 is a characteristic curve of op-amp common-mode rejection ratio, common mode rejection ratio is 82.3 dB, and the greater common mode rejection ratio shows that the design of amplifier has a high stability.

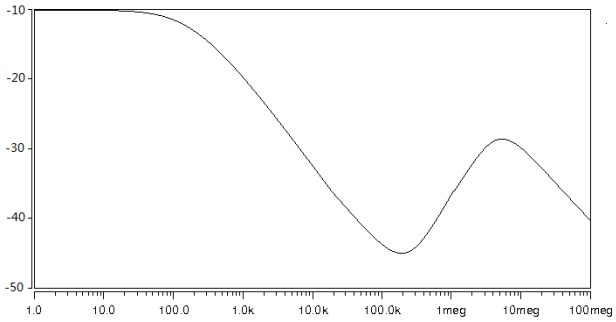


Figure 6 Op-amp common-mode rejection ratio.

## Conclusion

This paper studies High-performance folded cascode amplifier, overcomes the shortcomings of the Traditional folded cascode amplifiers and telescopic cascode amplifier, and it Has a high gain, low noise, high common mode rejection ratio and so on. To simulate and modulate by using simulation software, and consider with a number of design specifications, adjust width to length ratio of each MOS transistor, the simulation results meet the design requirements. This structure of folded cascode amplifier is simple and easy to implement, and suitable in the field of ADC interface circuit.

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# The research of programmable equivalent capacitor circuit

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**Abstract:** Resistors, inductors and capacitors are indispensable components in modern electronics field. While digital potentiometer is capable of conducting digital adjustments on resistances, the flexibility of adjusting the capacitance of most capacitors is still very limited even until now. This paper introduced a digital capacitor circuit based on impedance transformations. The impedance transformation circuit was set up by assembling an integrated operational amplifier and small amounts of resistors and capacitors. The capacitance of this circuit can be adjusted by controlling the resistance of a certain resistor using a digital potentiometer. Simulation results showed this circuit has many advantages including great flexibility if controlled with a single chip, wide capacitance adjustment range, insensitivity to temperature and pressure, and the size of the circuit remaining the same while the capacitance increases.

## Introduction

As the electronic technology develops, there are significantly increasing needs of digital programmable devices in this field. Now days, there are few digital adjustable capacitor products in the market. Most of available capacitors use simple analog switches to control the capacitance. This kind of capacitor has many disadvantages including size limitation and narrow adjustment range (only several to less than 20 pF). Also, most equivalent capacitor circuits consist of capacitors and resistors connecting in series or parallel instead of just capacitors alone. This narrows the freedom of the resistor in the circuit and subsequently limits the range of the equivalent capacitance. The digital capacitor introduced in this paper, using impedance changing circuit, yields pure capacitance equivalent outputs. In order to make the integration of the circuit easy, the traditional method of directly using analog switches to control the capacitance was abandoned. Instead, the capacitance was controlled by adjusting the resistance in the circuit. Using this method, the equivalent capacitance has large adjustable range and high accuracy, and the size of the equivalent circuit remains the same regardless the value of the capacitance output. This circuit, if adding a single chip to control the output capacitance, has the potential to be widely used in many different kinds of electronic devices.

## 1. Impedance generator principle

By impedance transformation of operational amplifier circuit is shown in figure 1.