Ingmar Kallfass

Comprehensive Nonlinear Modelling of Dispersive Heterostructure Field Effect Transistors and their MMIC Applications

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Ingmar Kallfass

aus Stuttgart

1. Gutachter:	Professor Dr.-Ing. Hermann Schumacher
2. Gutachter:	Professor Dr. Thomas J. Brazil
Amtierender Dekan:	Professor Dr.-Ing. Hans-Jörg Pfleiderer
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Contents

Introduction **1**

1 Modelled HEMT Technologies **4**
1.1 Strained-Si/SiGe mHEMT 4
1.2 Low Noise- and Power AlGaAs/GaAs pHEMT 9
1.3 InGaAs/InP pHEMT 11

2 Modelling of Frequency Dispersion in HFETs **13**
2.1 Physical- Versus Empirical Large-Signal Modelling 13
2.2 Effects of Frequency Dispersion in HFET Devices 16
2.3 State-of-the-Art Modelling Approaches 18
2.3.1 Thermal models 18
2.3.2 Static- and Dynamic Current Sources 19
2.3.3 Equivalent Voltage Sources 21
2.4 Importance of a Dispersion Model in Circuit Design 22
2.4.1 Static Analysis 22
2.4.2 Small-Signal Circuits 23
2.4.3 Large-Signal Frequency Domain Circuits 24
2.4.4 Large-Signal Time Domain Circuits 25
2.4.5 System Level 26
2.5 Obtaining Dynamic IV Characteristics 26
2.5.1 Pulsed-IV Characterisation 27
2.5.2 Numerical Integration of Dynamic Trans- and Output Conductance . 28

3 Universal Large-Signal HFET Model **33**
3.1 Advanced De-embedding Technique 33
3.2 Static Model 37
3.2.1 Modified COBRA drain current model 37
3.2.2 Gate current model 43
3.3 Dynamic Model 45
3.3.1 Multi-Bias Small-Signal Model Extraction 45
3.4 Nonlinear Capacitance Model 47

3.4.1 A Unified Approach to Charge-Conservative Capacitance Modelling . 48
3.4.2 A Universal HFET Capacitance Model 50
3.5 Multiple Time-Constant Dispersion Model 54
3.5.1 Physical Motivation 54
3.5.2 Single Time-Constant Dispersion Model 55
3.5.3 Multiple Time-Constants 57
3.5.4 Determination of Dispersion Time Constants 58
3.6 Parameter Extraction Software FETfit 66
3.7 Model Implementation 66
3.7.1 Implementation of nonlinear capacitance 69
3.7.2 Schematic level parameters 71
3.8 Small- and Large-Signal Model Verification 72

4 MMIC Applications 78
4.1 SiGe mHEMT Travelling-Wave Amplifiers 78
4.1.1 Transmission Line- and Active Device Models 79
4.1.2 Common-Source Stage Distributed Amplifier 80
4.1.3 Cascode Stage Distributed Amplifier 86
4.2 GaAs pHEMT Travelling-Wave Mixer and Variable Gain Amplifier 89
4.2.1 Unit Cell Topology and Operation Principle 89
4.2.2 Circuit Design and Layout 91
4.2.3 VGA Operation 92
4.2.4 Mixer Operation 98

5 Conclusion 102

Bibliography 105

List of Acronyms and Symbols 117

A Dynamic Small-Signal FET Model Equations 121

B Model Parameters, Equations and Derivatives 122

C Detailed Model Parameters and Verification 131
C.1 Strained-Si/SiGe mHEMT 131
C.2 Low-noise AlGaAs/GaAs pHEMT 136
C.3 Power AlGaAs/GaAs pHEMT 141
C.4 InGaAs/InP pHEMT 145

D SiGe mHEMT Two Metal Layers Process 150

Introduction

The Pseudomorphic High Electron Mobility Transistor (pHEMT) today is established as the prime transistor technology in analog front-ends of microwave and millimeter-wave applications. This is due to its up to date unrivalled capability of combining high cutoff frequencies with high power- and low noise performance. With the GaAs based device type offering highest maturity and availability, it is leading the microwave markets in wireless communication-, space-, defence- and automotive applications. In order to further improve cutoff frequencies and low noise performance, the metamorphic HEMT (mHEMT) concept has been developed, combining the advantages of a high In content in the channel region with GaAs substrates. Best performance, however, is reached in InP based pHEMT devices, which at the same time offer integrability with laser- and photo diode devices used in today's high-speed optical communication systems up to 80 Gbps. These well established technologies today are rivalled by potentially low-cost technologies, e.g. due to the improving power capability of high-speed SiGe heterojunction bipolar transistor (HBT) devices and the increased frequency performance of RF CMOS technologies, such as Silicon-on-Insulator (SOI) and strained-Si concepts. More recently, devices based on large bandgap materials like the GaN HEMT on SiC or Si substrates are entering high power markets like base stations in wireless communications. The mHEMT concept can also be applied to Si based devices by the introduction of strained-Si and strained-(Si)Ge channels formed on a SiGe buffer layer. This offers the potential of combining the high-frequency and low-noise HEMT performance with the ultra high integration density of conventional digital CMOS on the way towards the realisation of microwave System-on-Chip (SoC) applications.

A short time to market and prize competitiveness are the decisive factors for the success of products in the area of monolithic microwave ($f = 1...30\,\mathrm{GHz}$) and mm-wave ($f > 30\,\mathrm{GHz}$) integrated circuits (MMIC) and their systems. Therefore, an important element of the development chain of analog and mixed-signal ICs are accurate and efficient simulation models, enabling a reliable computer-aided design (CAD) prior to fabrication, and reducing or eliminating the need for costly and time-consuming redesign iterations. This is especially true for the III-V and advanced HEMT technologies, since they have to compete with the low-cost, high-volume Si-wafer based technologies mentioned above. Global validity in both the voltage operating domain as well as the frequency- and time domain qualifies a transistor model together with its computational efficiency when implemented into a simulation environment. In a comparison to purely physical and behavioural modelling approaches, the

compact, equivalent-circuit based models offer the best compromise between global validity, computational efficiency and adaptability to technology changes. The complex modulation schemes and stringent linearity requirements in modern electronic systems emphasize the need for such globally valid and efficient device models.

A particular challenge and area of research are frequency dispersive effects, present in all of the cutting-edge transistor technologies, due to effects of self-heating, carrier trapping and de-trapping, interface and surface charges as well as impact ionisation. On the device level, dispersion introduces a frequency- or time dependence to the current-voltage (IV) characteristics. Here, primarily the nonlinear drain current characteristics are concerned and most relevant for the overall device performance. On the circuit level, this has an impact on all of the major figures of merit in analog ICs. A dispersion model is required to accurately reflect both the static and the dynamic characteristics in MMICs.

This thesis presents a new custom model, universally applicable to dispersive HEMT transistors. The topics addressed cover areas from device characterisation and modelling, to the design and fabrication of MMIC applications. A novel theory for the inclusion of multiple time constant dispersion effects is developed and integrated into a nonlinear device model topology. Also, based on a novel unified approach to charge-conservative capacitance modelling, a nonlinear HEMT capacitance model is developed. An efficient drain current equation is employed to model both static and dynamic IV characteristics. The model, identical in topology and nonlinear functions, is fully extracted and validated for the following four different HEMT technologies:

- a 0.1 μm gate length strained-Si/SiGe mHEMT technology developed by Daimler-Chrysler Research,
- a 0.2 μm InP/InGaAs/InP pHEMT technology from Innovative Processing AG (IPAG),
- a commercial, state-of-the-art 0.15 μm AlGaAs/InGaAs/GaAs pHEMT high frequency, low-noise process, offered by United Monolithic Semiconductors (UMS) and
- the power version of the 0.15 μm GaAs pHEMT by UMS.

Based on the simulation model, which has been readily implemented into a conventional CAD environment, innovative MMIC applications with record performance have been successfully designed, fabricated and characterised.

In case of the strained-Si/SiGe mHEMT, the first full large-signal model has allowed for the successful realisation of the first and up to date only MMICs in this technology. A travelling-wave amplifier reaches 40 GHz with a gain of 4 dB.

Extraction and validation of the model for the InP pHEMT further proves the universal suitability of the adopted model topology and nonlinear functions, in particular the frequency dispersion part. The model is the first full large-signal model developed for this particular technology, enabling full circuit design and simulation capability.

As a supplement to the excellent foundry models of both the low-noise and the power version of the GaAs pHEMT, the presented model adds the dispersion capability as well as the more accurate nonlinear capacitance model. Travelling-wave MMICs have been realised in the power version of the GaAs pHEMT technology. A novel circuit concept is shown to act both as an ultra-broadband mixer and a variable gain amplifier (VGA). In excellent agreement with model prediction, a 2 dB conversion loss is reached within a bandwidth exceeding 50 GHz, while in amplifier mode, the gain can be controlled between 5...12 dB within a 43 GHz bandwidth.

Chapter 1

Modelled HEMT Technologies

This chapter deals with the different HEMT technologies which have been investigated by characterisation and model extraction. For all of them, a complete large-signal model including frequency dispersion has been developed.

Device performance related to the model extraction process is reviewed here. The discussion has a focus on electrical device characteristics and figures of merit (FOM). Technological issues are briefly discussed but extensively referenced only for the strained-Si/SiGe technology. For physics of the more conventional InP- and GaAs based devices as well as for basic HEMT operation theory, the reader is invited to refer to some of the excellent literature on this topic [1, 2, 3, 4]. Selected device physics will also be discussed in more detail in the section on frequency dispersion effects in chapter 2.2.

Special on-wafer modelling transistor samples with coplanar pad contacts and of varying gate size have kindly been provided by the respective device manufacturers. De-embedding techniques, described in detail in chapter 3.1, are employed to characterise and model the intrinsic HEMT devices.

1.1 Strained-Si/SiGe mHEMT

Strained-Si/SiGe Heterostructure Field-Effect Transistors (HFET) exploit the advantageous properties of the SiGe material system and its heterostructures to achieve significant speed improvement over conventional Si. Such devices can be realised in a variety of forms. Common to all concepts is the use of thin strained-Si or strained-(Si)Ge layers grown on top of a relaxed (virtual) substrate:

- Used as surface channel devices, one can realise n-channel and p-channel MOSFET structures. This concept has the prospect of significant speed enhancement to conventional CMOS and is therefore pursued by a number of major semiconductor companies, such as IBM [5, 6, 7], Intel, Philips and Atmel [8].

- In buried-channel devices, the principle of a two-dimensional electron- or hole gas (2DEG, 2DHG) in a quantum well is adapted to the $Si_{1-x}Ge_x$ material system. In

MOSFET-like devices with a gate dielectric layer, the channel is induced in a strained-Si layer by charge inversion. Technologically less complex devices use a channel which receives its carriers from donor layers on top and/or below, while the gate is typically formed by a metal-semiconductor (MS) or Schottky gate. Such devices are commonly designated as modulation-doped field-effect transistor (MODFET) or, in the case of n-channel devices, as HEMT. The buried-channel concept has the advantage of achieving higher cutoff frequencies due to reduced interface scattering. Also, being technologically less complex, it is more cost effective. SiGe MODFETs make use of strained-Si layers for n-type conduction or strained-(Si)Ge layers for p-type conduction. Such devices have been developed mainly by IBM [9, 10, 11, 12] and DaimlerChrysler Research [13, 14, 15] and have reached an impressive state of maturity. In Europe, in a close cooperation of several research groups, the development of the strained-Si/SiGe mHEMT approach has received support from several research projects, primarily the European Commission's SIGMUND [16] and Training and Mobility of Researchers (TMR) Network "SiGe Hetero Devices" [17] as well as the British EPSRC project SiGeMOS [18].

The formation of strained layers requires an underlying relaxed SiGe virtual substrate (VS). This in turn requires a buffer layer, grown on top of the Si substrate and allowing for lattice constant adjustment to the relaxed SiGe VS. Therefore, the device type is in principle a metamorphic one and hence designated as mHEMT in this work. To date, the realisation of these buffer layers is subject to intense research, motivated by the reduction of the necessary vertical layer thickness with the aim of achieving a flat topology favourable for a future integration of the SiGe mHEMT with standard Si CMOS. Several European groups are pursuing this aim employing different buffer technologies. In addition to the graded buffer using molecular-beam epitaxy (MBE), the approach used by DaimlerChrysler Research Ulm [19], techniques like low-temperature epitaxy (LTE) [20], low energy plasma enhanced chemical vapour deposition (LEPECVD) [21] and He-implantation assisted relaxation [22] are investigated.

Introducing alloys with Germanium into Si-based semiconductor devices offers various possibilities of improving the electrical performance of transistors. The difference in bandgap energy E_{g} of these two elements and their alloys allows for the realisation of hetero-interfaces in the conduction- and valence bands, a process often referenced as "bandgap-engineering". In the well-established SiGe HBT technology, for instance, the difference in bandgap energy in the base and emitter leads to a dramatic increase of current gain or emitter efficiency due to the suppression of reverse carrier injection from the base into the emitter. The MODFET, on the other hand, exploits the increased mobility of carriers when being spacially separated from their ionized donators/acceptors acting as scattering centers. In addition to mobility enhancement due to reduced scattering, one also exploits the significantly higher mobility of carriers in strained $\mathrm{Si}_{1-x}\mathrm{Ge}_x$ layers itself. The best mobility results are obtained for buried-channel devices (reduced interface scattering). For n-channel devices, record values

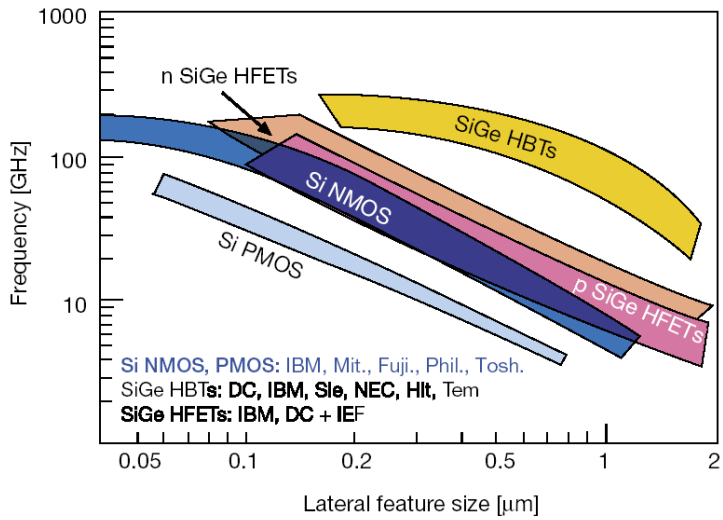

Figure 1.1: Maximum frequencies of oscillation of n- and p-channel SiGe HFETs compared to standard Si MOS and SiGe HBT, with respect to lateral device size. Source: [29].

of $\mu_n = 2800$ cm^2/Vs have been reported [23], an approximately six-fold increase to the universal electron mobility of inversion layers in Si [24][25]. In p-channel MODFETs, hole mobilities of $\mu_p = 3000\,\mathrm{cm}^2/\mathrm{Vs}$ have been achieved [26], representing an 18-fold increase to universal hole mobility in Si .

Fig. 1.1 shows the maximum frequencies of oscillation f_{max} of n- and p-channel SiGe MODFETs obtained from the main research groups compared to those of standard Si nMOS and pMOS as well as SiGe HBT technologies. The highest published results for the n-channel mHEMT type to date are $f_T = 90$ GHz and $f_{max} = 188$ GHz for the DaimlerChrysler device [27] and $f_T = 92$ GHz and $f_{max} = 212$ GHz for a recent IBM device [28].

In the SiGe mHEMT developed by DaimlerChrysler [30, 31] and employed in this work, a 2DEG is formed in a strained-Si quantum well, sandwiched between two Sb-doped SiGe supply layers. Obtaining a quantum well for electrons in the Si/SiGe material system is not so obvious, since it is well known from the SiGe HBT that the bandgap difference between Si and SiGe results in a valence band offset of almost the same magnitude $\Delta E_V \approx \Delta E_g$ and $\Delta E_C \approx 0$ eV [32]. An offset in the conduction band is achieved when the large bandgap Si material is strained. Then, a staggered or type-II hetero-interface is formed, generating the required conduction band quantum well for the HEMT channel [15, 33, 7]. All epitaxial layers are grown by MBE. In order to form a relaxed SiGe layer acting as VS, a relatively thick graded buffer is grown on the Si wafer. Fig. 1.2 shows the complete layer stack of the device, including the graded buffer, virtual substrate, active MBE layers as well as the HEMT structure. The 2 μm thick graded buffer has a final Ge content of 40 %.

In the frame of this work, the strained-Si/SiGe mHEMT has been extensively characterised in terms of its DC-, dynamic small- and large-signal- as well as microwave noise characteristics.

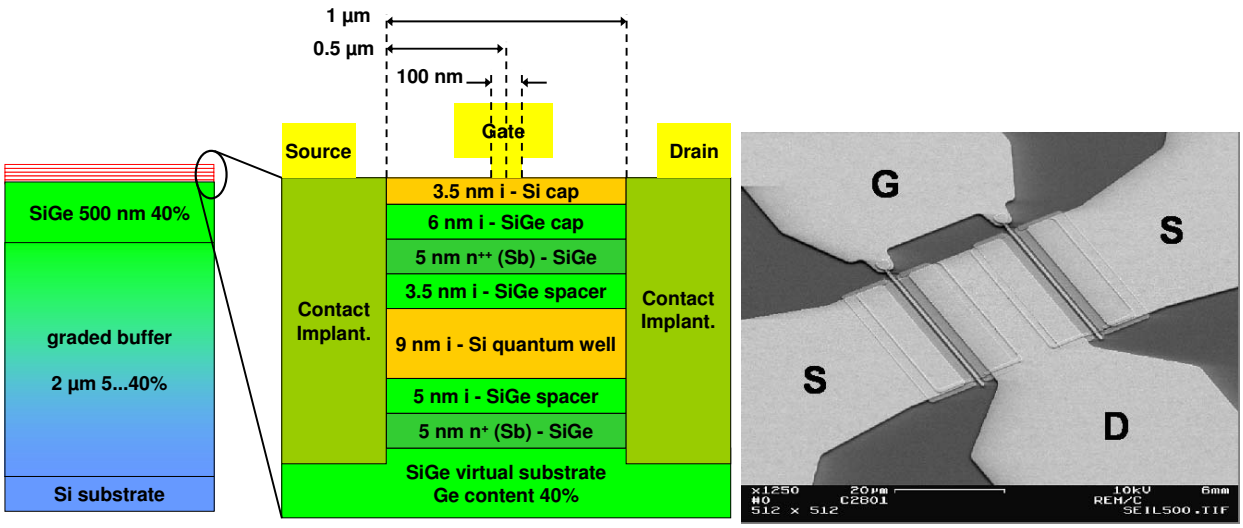

Figure 1.2: Left: Strained-Si/SiGe mHEMT layer stack including the virtual substrate- and epitaxial HEMT layers. Right: Device microphotograph with π-shaped gate structure.

Parameter	Symbol	Unit	Typical
Transition frequency	f_{T}	GHz	51
Maximum freq. of oscillation (via U)	f_{max}	GHz	101
Maximum transconductance (dynamic)	$g_{\mathrm{m,max}}$	mS/mm	250
Output conductance (dynamic)	g_{ds}	mS/mm	13
Optimum gate-source voltage ($g_{\mathrm{m,max}}$)	$V_{\mathrm{gs,opt}}$	V	-0.3
Optimum drain current ($g_{\mathrm{m,max}}$)	I_{dss}	mA/mm	75
Threshold voltage	V_{t}	V	-0.7
Drain-source breakdown voltage	V_{bds}	V	3.5

Table 1.1: Strained-Si/SiGe mHEMT figures of merit.

Fig. 1.3 shows the extrapolation of f_{T} and f_{max} under maximum gain conditions in a $2 \times 50\,\mu$m gate width, $0.1\,\mu$m gate length strained-Si/SiGe mHEMT. Typical measured cutoff frequencies are $f_{\mathrm{T}} = 51$ GHz and $f_{\mathrm{max}} = 101$ GHz. Fig. 1.3(right) plots cutoff frequencies versus drain voltage. f_{T} doesn't drop significantly down to very low voltages of about $V_{\mathrm{ds}} = 0.4$ V. This is the reason why, recently, the SiGe mHEMT's advantages in the field of low-power applications have been investigated [34, 35].

Fig. 1.4 shows the minimum noise figure F_{min} together with associated gain G_{ass}. The device achieves as low as 1.8 dB noise at 24 GHz, important e.g. for applications in this ISM (industrial-scientific-medical) band. In the Ku-band, a noise figure of about 0.5 dB is achieved with a respectable associated gain of 11.9 dB. Optimum bias for low-noise operation is $V_{\mathrm{gs}} = -0.3$ V and $V_{\mathrm{ds}} = 2.5$ V. The right plot of Fig. 1.4 shows cutoff frequencies versus gate voltage. The voltage regime for high f_{T} extends well down to low gate bias, where low noise operation occurs.

Table 1.1 lists the main figures of merit of the strained-Si/SiGe mHEMT.

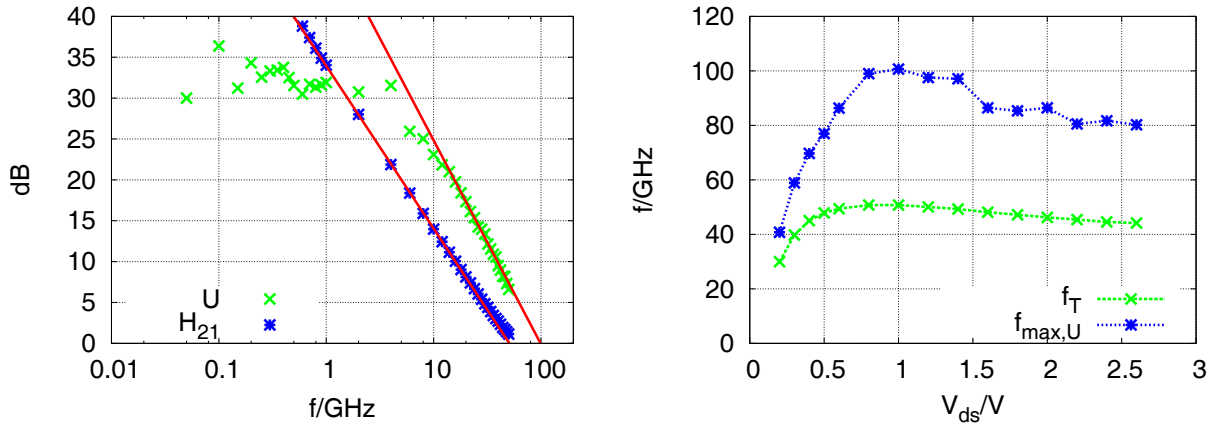

Figure 1.3: Extrapolation of f_{T} and $f_{\max}$ in a 2x50 μm strained-Si/SiGe mHEMT (left). The plot of cutoff frequencies versus drain voltage shows the device's suitability for low-power operation (right).

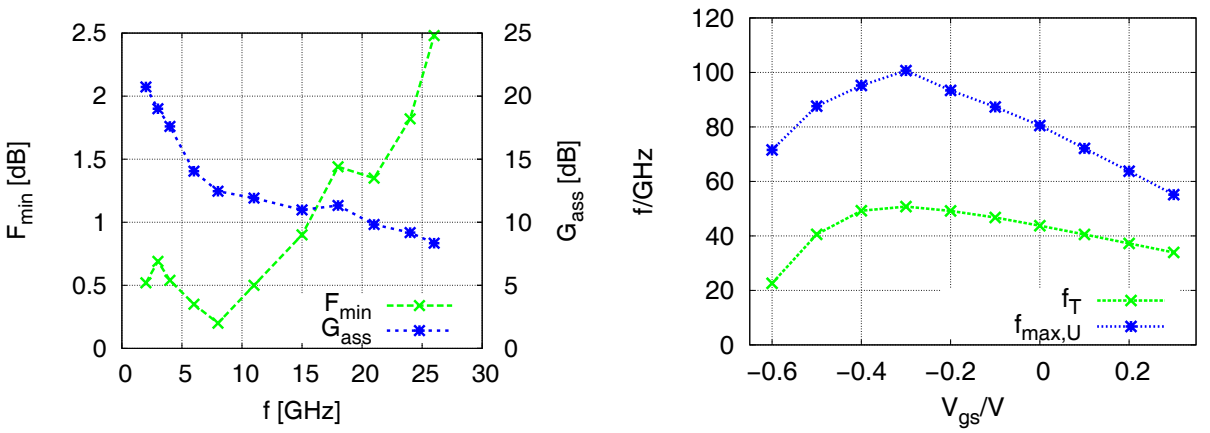

Figure 1.4: F_{min} and G_{ass} in a $2 \times 50\,\mu$m strained-Si/SiGe mHEMT versus frequency (left). Plotting cutoff frequencies versus gate voltage reveals that high gain is achieved together with low noise (right).

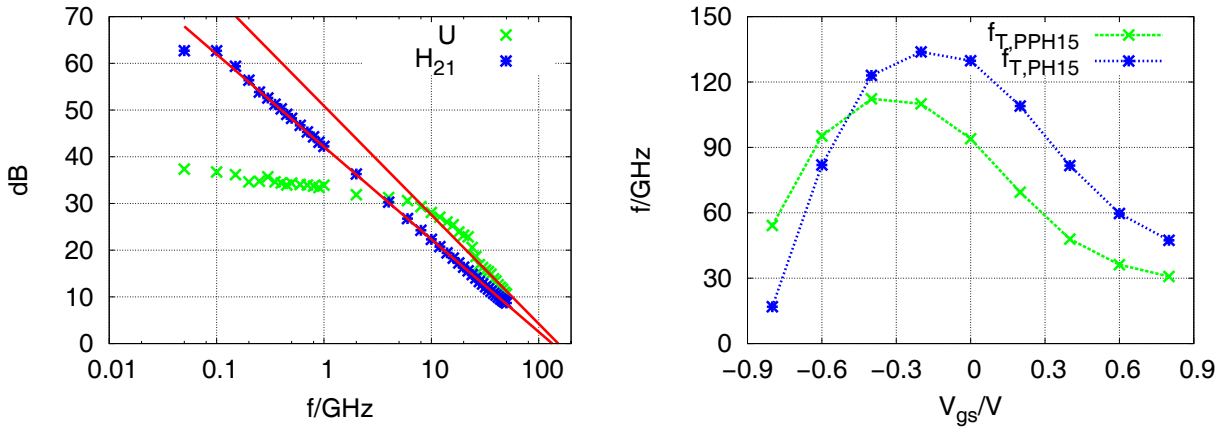

Figure 1.5: Extrapolation of f_{T} and $f_{\max}$ in a 2x50 μm PH15 device (left). Comparison of PH15- and PPH15 transition frequency versus gate voltage (right).

This performance data together with the achieved technological maturity and reproducibility recommend the strained-Si/SiGe mHEMT for the realisation of microwave and mm-wave applications. The device offers high cutoff frequencies with low-noise and adequate power capabilities. Previous modelling work concentrated on physical and small-signal model extraction [36, 37]. The developed model in this work is the first full large-signal model for the SiGe mHEMT together with the rigorous investigation and modelling of frequency dispersion. Its implementation in a circuit design environment has enabled the design and realisation of the first Si/SiGe MMIC applications [38, 39].

1.2 Low Noise- and Power AlGaAs/GaAs pHEMT

On-wafer transistor samples of the commercial 0.15 μm gate length GaAs pHEMT process "PH15" from UMS are used for characterisation and model extraction. The PH15 process is optimised for low noise- and high frequency performance of its active devices. This very mature and optimised technology reaches a measured f_{T} of 134 GHz and $f_{\max}$ of 152 GHz. The power variant of the 0.15 μm GaAs pHEMT process from UMS is abbreviated as PPH15. The process trades a reduction in the cutoff frequencies with $f_{\mathrm{T}} = 112\,\mathrm{GHz}$ and $f_{\max} = 97\,\mathrm{GHz}$ for a high breakdown voltage of $V_{\mathrm{bds}} = 8\,\mathrm{V}$. This is achieved by introducing double supply layers, i.e. delta-doping is used both below and on top of the InGaAs quantum well [40]. Doping levels are reduced compared to the single-supply of the PH15 process, resulting in higher breakdown voltage. Fig. 1.5 shows the comparison of f_{T} versus gate voltage for PH15 and PPH15. Both the maximum value and the gate voltage for maximum gain are shifted. Table 1.2 shows selected figures of merit for the PH15- and PPH15 pHEMT technologies.

Fig. 1.6 shows a microphotograph of a $4\,\mathrm{x}\,75\,\mu$m PPH15 transistor sample in common-source configuration. In addition to being grounded by via holes, the source contacts are