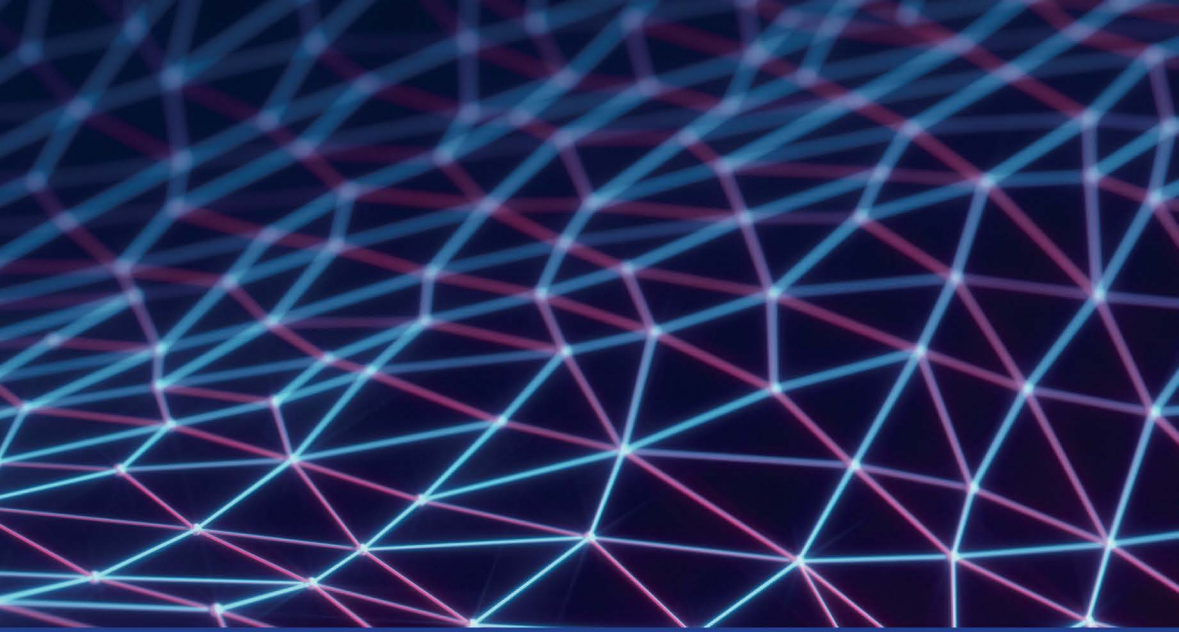

INTEGRATED CIRCUIT FABRICATION

Kumar Shubham and Ankaj Gupta

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Integrated Circuit Fabrication


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To Our Parents

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Family


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Brief Contents


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Detail Contents

Preface

The book for students in engineering and technology curricula. It is a comprehensive treatment of integrated circuit fabrication. This text will be very useful to every student and practicing professional dealing with fabrication process. It covers theoretical and practical aspects of all major steps in the fabrication sequence. This book can be used conveniently in a semester length course on integrated circuit fabrication. This text can also serve as a reference for practicing engineer and scientist in the semiconductor industry.

IC Fabrications are ever demanding of technology in rapidly growing industry where growth opportunities are numerous. A recent survey shows that integrated circuit currently outnumbers humans in UK, USA, India and China. The spectacular advances in the development and application of integrated circuit technology have led to the emergence of microelectronic process engineering as an independent discipline.

Integrated circuit fabrication text books typically divide the fabrication sequence into a number of unit processes that are repeated to form the integrated circuit. Most students have difficulty recalling all of the background material. They have seen it once, two or three years and many final exams ago. The effect is to give the book a analysis flavor: a number of loosely related topics each with its own background material. It is vital that this fundamental material be re-established before students take up new material.

Manuscript Organization

Chapter 1 presents brief historical overview of major semiconductor devices and vital technological development, as well as introduction to basic fabrication step. Introduces crystal growth and process to obtain single crystal of silicon.

Chapter 2 deals with epitaxy. The purpose of epitaxy is to grow a silicon layer of uniform thickness and accurately controlled electrical properties and so to provide a perfect substrate for the subsequent device processing.

Chapter 3 presents silicon oxidation. It refers to the conversion of the silicon wafer to silicon oxide (SiO_2 or more generally SiOx). The ability of Si to form an oxide layer is very important since this is one of the reasons for choosing Si over Ge.

Chapter 4 discuss lithography. It is the process of transferring patterns of geometric shapes in a mask to a thin layer of radiation-sensitive material (called resist) covering the surface of a semiconductor wafer.

Chapter 5 explain the process of etching that explain dry and wet etching process of different materials.

Chapter 6 refers diffusion to the entire process of adding a dopant to the surface of wafer at high temperature.

Chapter 7 discuss ion-implantation which replaces diffusion process in IC fabrication for reliable and reproducable doping.

Chapter 8 presents Film Deposition which contains two part Dielectric film deposition and metallization. It contains SiO_2 and Si_3N_4 film deposition which act as passivative material in IC. Metallization refers to the metal layers that electrically interconnect the various device structures fabricated on the silicon substrate. Thin-film aluminum is the most widely used material for metallization, and is said to be the third major ingredient for IC fabrication, with the other two being silicon and SiO_2.

Chapter 9 deals with packaging. It is final stage of IC fabrication. In this the tiny block of semiconducting material is encapsulated in a supporting case that prevents physical damage and corrosion.

Chapter 10 is all about VLSI process integration. It presents fundamentals of integrating silicon processing steps to create silicon devices.

In this text over 400 references have been cited, of which 30 percent were published in last ten years, and over 200 technical illustrations are included, of which 45 percent are new. The problems at the end of each chapter form an integral part of the development of the topic. We have also attempted in each chapter to conclude some discussion of future trends. This book is organized somewhat differently than other texts on this general topic.

Suggestions for further improvements of the book will be gratefully acknowledge.

Authors

1

Introduction to Silicon Wafer Processing

1.1 INTRODUCTION

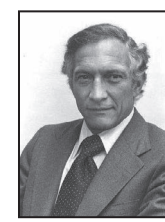
Designing a complex electronic machine of compact size like a laptop or mobile, it is always desired and necessary to increase the number of components involved in order to make technical advanced. The logic operation parts of the machines are conducted through integrated circuits made of semiconductor material. The monolithic integrated circuit placed the previously separated diodes, transistors, resistors, capacitors and all the connecting wiring onto a single crystal (or 'chip'). The monolithic integrated circuit was fated to be invented as two inventors who were unaware of each others activities, invented almost identical integrated circuits or ICs at nearly the same time.

Jack Kilby, an engineer from Texas Instruments in 1958 with a background in ceramic-based silk screen circuit boards and transistor-based hearing aids had similar idea of making a whole circuit on a single chip as of research engineer Robert Noyce who had co-founded the Fairchild Semiconductor Corporation in 1957.

What we didn't realize then was the integrated circuit would reduce the cost of electronic functions by a factor of a million to one, nothing had ever done that for anything before" – Jack Kilby

In 1961 the first commercially available integrated circuits came from the Fairchild Semiconductor Corporation.

Jack Kilbe



Robert Noyce

Fig. 1.1 Photo image of (a) Jack Kilbe (b) Robert Noyce

Jack Kilby holds patents on more than sixty inventions and is also well known as the inventor of the portable calculator (1967), awarded the National Medal of Science in 1970. Robert Noyce, with sixteen patents to his name, founded Intel, the company responsible for the invention of the microprocessor, in 1968. The invention of the integrated circuit by both men stands historically as one of the most important innovations of mankind as almost all modern products use chip technology. Kilby used Germanium and Noyce used silicon for the semiconductor material.

All computers then started to be made using chips instead of assembling the individual transistors and their accompanying parts. Texas Instruments first used the chips in Air Force computers and the Minuteman Missile in 1962. They later used the chips to produce the first electronic portable calculators. The first IC had only one transistor, three resistors, and one capacitor having a size of an adult's pinkie finger. Today an IC smaller than a penny can hold more than 1 billion transistors.

The advantages of integrated circuits are as follows

1. Small in size due to the reduced device dimension
2. Low weight due to very small size
3. Low power requirement due to lower dimension and lower threshold power requirement
4. Low cost due to large-scale production and cheap material
5. High reliability due to the absence of a solder joint
6. Provide facilitation to integrate large number of devices and components.
7. Improves the device performance even at high-frequency region

The disadvantages of integrated circuits are as follows

1. IC resistors have a limited range
2. Due to bulky size generally inductors (L) cannot be formed using IC
3. Transformers cannot be formed using IC.

1.2 VLSI GENERATIONS

Historically, the first semiconductor IC chips held one transistor with three resistors and one capacitor. Advancement of technology enabled us to add more and more number of transistors.

The first to arrive was Small-Scale Integration (SSI), then improvements in technique led to devices with millions to billions of logic gates–Very Large-Scale Integration (VLSI).

Present day's microprocessors have millions of logic gates and transistors. Intel co-founder, Gordon E. Moore, in 1965 published a paper on the future projection of IC technology.

Moore's Law is responsible for "smaller, compact, cheaper and more efficient IC". Gordon Moore's empirical relationship is cited in a number of forms, but its essential thesis is that the numbers of transistors that can be manufactured on a single die will double every 18 months.

Wickes (1969) in his paper categorizes between SSI, MSI and LSI by the number of logic gates implemented on single chip where single equivalent logic gate is taken as the fundamental building block. On this basis a SSI circuit is one which has 1~10 equivalent logic gates, an MSI circuit is one which has 10~100 logic gates and LSI circuit is one which has more than 100 logic gates. (e.g., random access bipolar memory modules have approximately 500 equivalent gates and other advanced modules are expected to have four times the number.) After the success of LSI, the era of Very Large Scale Integration (VLSI), Extra Large Scale Integration (ELSI), Ultra Large Scale Integration (ULSI), etc has begun with having the ability to perform a very complex logic function, or a large number of simple logic functions in very short time.

The first generation integrated circuits contained only a few transistors called "Small-Scale Integration" (SSI), they used circuits containing transistors numbering in the tens.

SSI circuits were used in early Aerospace project and Missile projects. The two major program of that time, Minuteman missile and Apollo program needed lightweight digital computers for their inertial guidance systems. The Apollo guidance computer motivated the integrated-circuit technology, while the Minuteman missile forced it into mass-production which led SSI to become commercial. These programs acquired almost all of the available integrated circuits from 1960 through 1963, and almost alone provided the demand that funded the production improvements to get the production costs from $1000/circuit (in 1960 dollars) to merely $25/circuit (in 1963 dollars). After the successful implementation in defense industry they began to appear in consumer products a typical application being FM inter-carrier sound processing in television receivers.

In the late 1960s, the next step in the development of integrated circuit was taken with introduction of devices that contained hundreds of transistors on each chip, called Medium-Scale Integration" (MSI).

They were more attractive and fast processing then SSI because, they allowed more complex systems to be produced using smaller circuit boards, less assembly work (because of fewer separate components), and a number of other advantages but they cost little more to produce than SSI devices.

First and second generation microprocessor, computer memories, calculator chips led further development of IC for mass commercial production so Large Scale Integration (LSI) circuits come into picture in the early 1970s that contain tens of thousand transistors on each chip and finally in 1974 to Very Large Scale Integration (VLSI) circuits containing hundreds of thousands transistors on each chip in early 1980s and continues to millions transistors. This led to increase production of chips utilizing then in different new products also the shrinking of chip size and reduction of chip cost.

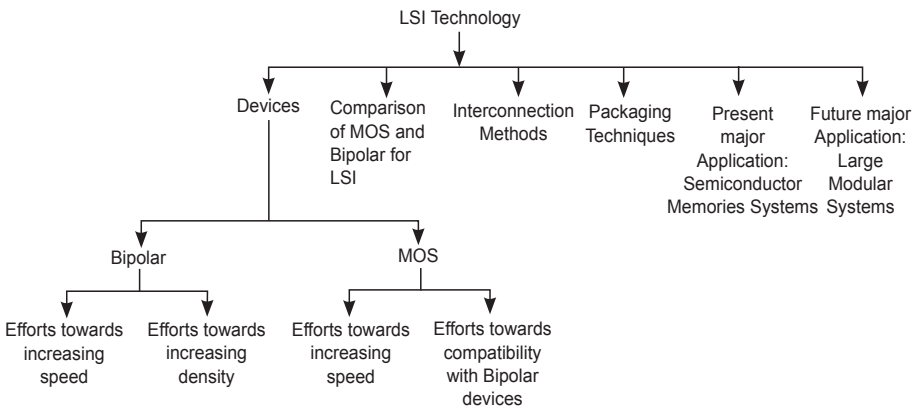


Fig. 1.2 LSI Technology

Figure 1.2 gives the way of dividing discussion on LSI technology on a number of dimensions.

Scale of Integration	No of Transistor	Function	Time
SSI	Fewer than 10	Input and output gates are connected directly to package	1963
MSI	10 to 99	Performs digital function like decoders, adders, registers	1970
LSI	100 to 9999	Includes digital systems such as processors, memory chips and programmable modules	1975
VLSI/ULSI	10000 to 99999	Include large memory array and complex microcomputer chips	1980

In recent years the rate of growth has showed difficulties in defining, designing and processing complicated chips were about 100 million devices /chip available before 2000 and 1 billion in 2011. The devices which are used in today's integrated circuits, primarily CMOS, Bi-CMOS, GaAs and FinFET, in 1980 at the beginning of VLSI era the minimum feature size was 2μm which shrink to 0.1 μm in 2000 and to 0.022μm in 2011. Device miniaturization results in reduced unit cost per function and in improved performance. The device speed has improved by four orders of magnitude since 1960. Higher speed leads to expanded IC functional throughput rates. Digital ICs are able to perform data processing, numerical computation and signal conditioning at 10 and higher gigabit per second rates. Another benefit is the reduction of power consume as the device become smaller so, consume less power and reduces the energy used for each switching operation.

1.3 CLEAN ROOM

In 1965 the chip manufacturing factories were filthy by today's standards and wafer cleaning procedures were unorganized having poorly understood. The chips were manufactured in those days when they were very small, unreliable and contained very few components by today's standards. Defects on a chip tens to reduce yields exponentially as chip size increases, small chip can be manufactured even in quite dirty environment.

The semiconductor devices are fabricated by introducing dopants, often at concentrations of parts per billion and by depositing and patterning thin films on the wafer surface, often with a thickness control of a few nano meter (nm). Such processes are fabricated and reproducible with high accuracy only if stray contaminants can be held to levels below those that affect devices characteristics on chip yield. Modern IC manufacturing units employ clean rooms to control unwanted impurities. Clean room is implemented by building the chips in a clean dust free ambiance having highly filtered air. Apparatus are designed to minimize particle and residual production for that ultra-pure chemicals and highly filtered gases are used.

The numerous developments have been made in shrinking device geometry refer as device miniaturization and in improving manufacturing so that larger chips can be economically built. This development requires that defect control associated within the manufacturing process also improve. The Semiconductor Industry Association (SIA) data has been summarized in Table 1.1.

Table 1.1 Implication of Semiconductor Industry Growth on defect size, density and contamination level

Year of DRAM shipment	1999	2003	2006	2009	2012	2015
Critical defect size	90 nm	65 nm	50 nm	35 nm	25 nm	18 nm
Starting wafer total LLS (cm^{-2})	0.29	0.14	0.06	0.03	0.015	**0.05**
DRAM GOI defect density (cm^{-2})	0.03	0.014	0.006	0.003	0.001	**0.001**
Logic GOI defect density (cm^{-2})	0.15	0.08	0.05	0.04	0.03	**0.01**
Standard Wafer total bulk Fe (cm^{-2})	$1*10^{10}$	Under $1*10^{10}$	Under $1*10^{10}$	Under $1*10^{10}$	Under $1*10^{10}$	Under $1*10^{10}$
Critical metals on wafer surface after cleaning (cm^{-2})	$4*10^{9}$	$2*10^{9}$	$1*10^{9}$	$< 10^{9}$	$< 10^{9}$	$< 10^{9}$
Starting Material Recombination Lifetime (μ sec)	>=325	>=325	>=325	>=450	>=450	>=450

It is obvious that great care must be taken in making sure that the factories in which chips are manufactured are as clean as possible. Even with a ultra clean environment, and even with procedure with clean wafers thoroughly and often, it is not realistic to expect that all impurities can be kept out of silicon wafers. The critical particle size of the impurity/dopant/dust is on the order of half of the minimum feature size of the devices. Particles larger than this size have a high probability of causing a manufacturing defect. There is simply too much processing and handling of the wafers during IC fabrication.

The manufacturing units producing chips must have clean facilities. Particles that might deposit on a silicon wafer and cause a defect may originate from many sources including people touch-dust, machines processing chemicals, process and residual gases. Such particles may be airborne or may be suspended in liquids or gases. It is common to characterize the cleanliness of air in IC facilities by the designation "class 10 or class 100". Figure 1.3 illustrates the meaning of these terms.

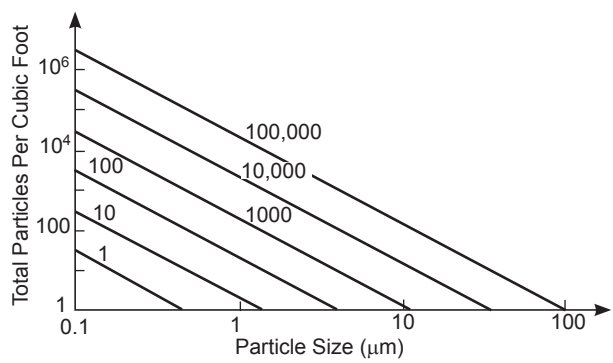


Fig. 1.3 Particle size distribution curve for various classes of clean room. The vertical axis is the total number of particles larger than a given particle size.

Class 10 classifies that in each cubic foot of air in the manufacturing unit, there are less than 10 total particles having size greater than 0.5 μm. A typical class room of university is about class 100000 while room air in state of the art manufacturing facilities today is typically class 1 in critical areas. This level of cleanliness is obtained through a combination of air filtration and circulation, clean room design and through careful elimination of particular sources.

Particles in the air in a manufacturing plant generally come from several main sources. This includes the people who work in the plant, machines that operate in the plant, and supplies that are brought into the plant. Many studies have been done to identify particle source and the relative importance of various sources. For example people typically emit several hundred particle per minute from each cm^2 of surface area. The actual rate is different for clothing versus skin versus hair but net result is that a typical human emits 5-10 million particles per minute. Most modern IC manufacturing plant makes use of robots for wafer handling in an effort to minimize human handling and therefore particle contamination.

The very first step in reducing particles is to minimize these sources. People in the plant should wear "bunny suits" which cover their bodies and clothing and which lock particle emissions from these sources. Face masks and individual air filters are also worn to prevent exhaling particles into the room air. Few minute air showers at the entrance of the clean room to blow loose particles off from people before they enter as well as clean room protocols are enforced to minimize particle generation. Machines those handles the wafers in the plant are specifically designed to minimize particle generation and materials are chosen for use inside the plant which minimize particle emission.

The source of particles can never be completely eliminated but constant air filtration is used to remove generated particles. This is accomplished by recirculating the air through High Efficiency Particulate Air (HEPA) filters. These filters are composed of thin porous sheets of ultrafine glass fibers (< 0.5 μm diameter). Room air is forced through the filters with a velocity of about 50 cm/sec. large particles are trapped by the filters; small particles impact the fibers as they pass through the filter and stick to these fibers primarily through electrostatic forces. The net results of HEPA filters are 99.98% efficient at removing particles from the air.

Most IC manufacturing facility produces their own clean water on site, starting with water from the local water supply. This water is filtered to remove dissolved particles and organics. Dissolved ionic species are removed by ion exchange or reverse osmosis. The result is high purity (high resistivity in MΩ) water that is used in large quantities in the plant.

Modern Chip manufacturing plant is designed to continuously recirculate the room air through HEPA filters to maintain a class 10 or class 1 ambiance. A typical clean room is shown in figure 1.4.

Fig. 1.4 Typical modern cleanroom for IC fabrication.
(Photo courtesy of graphene.manchester.ac.uk)

All mechanical support equipment is located beneath the clean room to minimize contamination from these machines. The HEPA filters are located in the ceiling of clean room. The fans that recirculate the air are normally placed above HEPA filter. Inside cleanroom, finger walls or chases provide a path for air return as well as to bring in electric power, distilled water and gases. The scientist and engineers wear " bunny suits" to minimize particle emission.

1.4 SEMICONDUCTOR MATERIALS

Semiconductors are a class of materials which have the unique properties that their electrical conductivity can be controlled over a very wide range by the introduction of dopants. Dopants are atoms that generally contain either one more or one fewer electrons in their outermost shell than the host semiconductor. They provide one extra electron or one missing electron (a "hole") compared to the host atoms. These excess electron and holes are the carriers which carry current in semiconductor devices. The key to building IC lies in the ability to control the local doping and hence the local electronic properties of semiconductor crystal.

Elemental semiconductors all of which have covalent bonding or sharing arrangement in essence populates the entire outer shell for each atom, resulting in a stable structure in which all electron are bound to atoms at least at very low temperature. This kind of bonding arrangement lies in column IV of

periodic table shown in figure 1.5. This same type of bonding arrangement can be produced using mixture of elements from other columns of periodic table known as compound semiconductors. For example GaAs consists of alternating Ga (Column III) and As (Column V) atoms which have an average of four electron per atom, ZnO consist of alternating Zn (Column II) and O (column VI) atoms which have an average of four electron per atom and so the same covalent bonding arrangements works. More complex examples like, $Al_xGa_{1-x}As$, $Hg_xCd_{1-x}Te$, $Al_{1-x}Ga_xAs_yP_{1-y}$ are also possible. Thus nature provides many possible materials which can act as semiconductor.

	III	IV	V	VI
	5 **B** 10.81	6 **C** 12.01	7 **N** 14.01	8 **O** 16.00
	13 **Al** 26.96	14 **Si** 28.09	15 **P** 30.97	16 **S** 32.06
30 **Zn** 65.38	31 **Ga** 69.72	32 **Ge** 72.59	33 **As** 74.92	34 **Se** 78.96
48 **Cd** 112.40	49 **In** 114.80	50 **Sn** 118.70	51 **Sb** 121.80	52 **Te** 127.60

Fig. 1.5 Periodic table portion relevant for elemental and compound Semiconductors

At temperature above absolute zero thermal energy can break some of the covalent bond of semiconductor which creates both a free or mobile electron and a mobile hole. The concentration of electron and holes are exactly equal in pure semiconductor are referred to as intrinsic semiconductor. The conductivity of pure semiconductor depends on the broken covalent bond due to temperature. So the free charge carriers are very few in pure semiconductor. Fortunately semiconductors have the properties that they can be doped with other materials. Doping results in a column V (P, As) or a column III (B, Al) atom replacing a semiconductor atom in the crystal structure. Such dopants either contribute an extra electron (column V) to the crystal, become N-type dopants or they contribute a hole (column III), become p-type dopants. The electron and holes are introduced on a one for one basis by the dopants. Doping could be accomplished by diffusion or ion-implantation, modern IC technology generally uses ion-implantation to dope semiconductor which permits controlled introduction of parts per million to parts per hundred of dopant atoms. As a result conductivity of semiconductor can be controlled over a very wide range, permitting many types of semiconductor devices to be

fabricated. The device fabrication involve a large processing steps. Elemental semiconductors (Si, Ge) have advantages over compound semiconductor as they do not decompose on processing. Although Silicon (Si) dominate (about 95%) in semiconductor industry but it is not an optimum choice in every respect. For optoel ectronic purpose Si is not preferred as it is indirect bandgap semiconductor. For this compound semiconductor of direct bandgap is preferred such as GaAs. Which processing technology is most highly developed. There are several reasons for Si to become the preferred elemental semiconductor for IC in the present over Ge. The reasons are listed below as:

1. Si has a larger bandgap (1.1eV) compared to Ge (0.7eV) at room temperature) and because of this the henomenon of thermal electron hole pair generation is smaller in Si then Ge. Which mean that at the same temperature the noise of the Si devices is smaller than the noise of Ge devices.
2. Si is relatively easy and inexpensive to obtain and process so it is cheap whereas Ge is rare material that is typically found with copper, lead or silver deposits so it is expensive and difficult to process comparatively.
3. Unlike Ge, Si forms native oxide (thin layer of SiO_2) on its surface very easily which is a very good insulator and which technologically can be very easily processed. Thin layer of oxide is very useful to form the gates of MOSFET transistors. Ge does not form native oxide layer on its surface so easily and technology to obtain the Ge devices is more complicated.
4. The reverse current in Si flows in order of nano-amperes compared to Ge in which the reverse current in order of micro-amperes because of this the accuracy of non-conduction of Ge diode in reverse bias falls down. The Si diode has large reverse breakdown about 70-100 V compared to Ge which has the reverse breakdown voltage around 50 V.
5. Because of the high band gap temperature stability of Si is good, it can withstand in temperature range typically 140°C to 180°C whereas Ge is much temperature sensitive only upto 70°C.

1.5 CRYSTAL STRUCTURE

The materials used for microelectronics can be divided into three classifications (Amorphous, Single crystal & Poly crystal), depending on the amount of atomic order they possess.

In single crystal materials, almost all of the atoms in the crystal occupy well-defined and regular positions known as lattice sites. In semiconductor products

base layer is single crystal provided by the wafer or substrate. If there is an additional single-crystal layer, it is grown epitaxially on substrate.

Amorphous materials are at the opposite extreme the atoms have no long-range order such as SiO_2. Instead, the chemical bonds have a range of lengths and orientations.

The third class of materials is polycrystalline. These materials are a collection of small single crystals randomly oriented with respect to each other. The size and orientation of these crystals often change during processing and sometimes even during circuit operation.

The silicon industry depends on a ready supply of high quality single crystal wafers.

Crystals are described by their most basic structural element a "unit cell" simply arranged in an array, repeated in a very regular manner over three dimensions. The unit cells of interest have cubic symmetry with each edge of the unit cell being the same length.

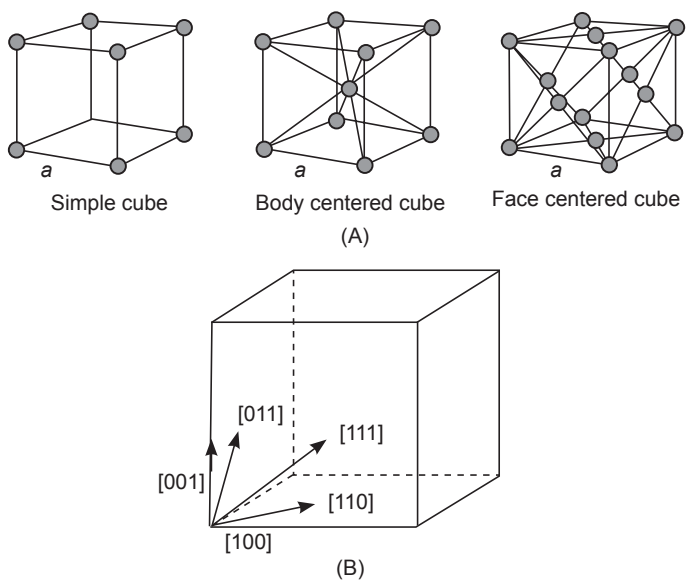


Fig. 1.6 (a) Cubic Crystal lattices b) Crystal orientation in cubic system

Figure 1.6 shows three simple crystal unit cells. All are based on a cubic structure.

Simple Cubic (SC): Polonium crystal exhibits this structure over a narrow range of temperature. The SC cell has atoms at the corners of the cell.

Body Centred Cubic (BCC): Molybdenum, tentalum and tungsten exhibits this crystal. The bcc cell has an additional extra atom in the center of the cube than SC.

Face-Centred Cubic (FCC): This structure is exhibited by a large number of elements such as copper, gold, nickel, platinum and silver. This cell has additional extra atoms in the center of each face of the cube than SC.

The directions in a crystal are identified using a Cartesian coordinate system as [*x,y,z*].For a cubic crystal, the faces of the cell form planes that are perpendicular to the axes of the coordinate system. The symbol (*x,y,z*) is used to denote a particular plane that is perpendicular to the vector that points from the origin along the [*x,y,z*] direction. Figure 1.6 b) shows several common crystal directions. The set of numbers *h,k*, and *l* that are used to describe planes in this manner are called the *Miller indices* of a plane. They are found for a given plane by taking the inverse of the points at which the plane in question crosses the three coordinate axes, then multiplying by the smallest possible factor to make *h, k*, and *l* integers. The notation {*h,k,l*} is also used to represent crystal planes. This representation is meant to include not only the given plane, but also all equivalent planes. For example, in a crystal with cubic symmetry the (100) plane will have exactly the same properties as the (010) and (001) planes. The only difference is an arbitrary choice of coordinate system and the notation {100} refers to all three.

Silicon and germanium are both group IV elements. They have four valence electrons and need four more to complete their valence shell. In crystals, this is done by forming covalent bonds with four nearest neighbor atoms. None of the basic cubic structures in figure 1.6 would therefore be appropriate. The simple cubic crystal has six nearest neighbors, the body-centered cubic (BCC) has eight, and the face-centered cubic (FCC) has twelve. Instead, group IV semiconductors form in the diamond structure shown in figure 1.7. The unit cell of Si can be constructed by starting with an FCC cell and adding four additional atoms If the length of each side is *a*,the four additional atoms are located at (*a*/4, *a*/4, *a*/4), (3*a*/4, 3*a*/4, *a*/4), (3*a*/4, *a*/4, 3*a*/4), and (*a*/4 3*a*/4, 3*a*/4).

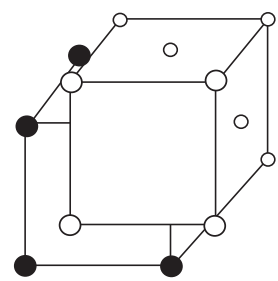


Fig. 1.7 Zincblende Lattice

This crystal structure can also be thought of as two interlocking FCC lattices. Gallium arsenide also forms in this same arrangement; however, when two elements are present, the crystal has a reduced level of symmetry so the structure is then called zincblende.

1.6 CRYSTAL DEFECTS

A perfect crystal that has every atom of the same type in the correct position does not exist. All crystals have some defects which contribute to the mechanical properties of materials. In fact, using the term "defect" is sort of a misnomer since these features are commonly intentionally used to manipulate the mechanical properties of a material as adding alloying elements to a metal is one way of introducing a crystal defect. Nevertheless, the term "defect" will be used to just keep in mind that crystalline defects are not always bad. Semiconductor wafers are highly perfect single crystals. There are several types of defects which are commonly found in crystals. Nevertheless, crystal defects play an important role in semiconductor fabrication. Semiconductor defects or imperfections, can be distributed into four types depending on their dimensionality as describe in figure 1.8. These are

- Point defect
- Line defect
- Area defect
- Volume defect

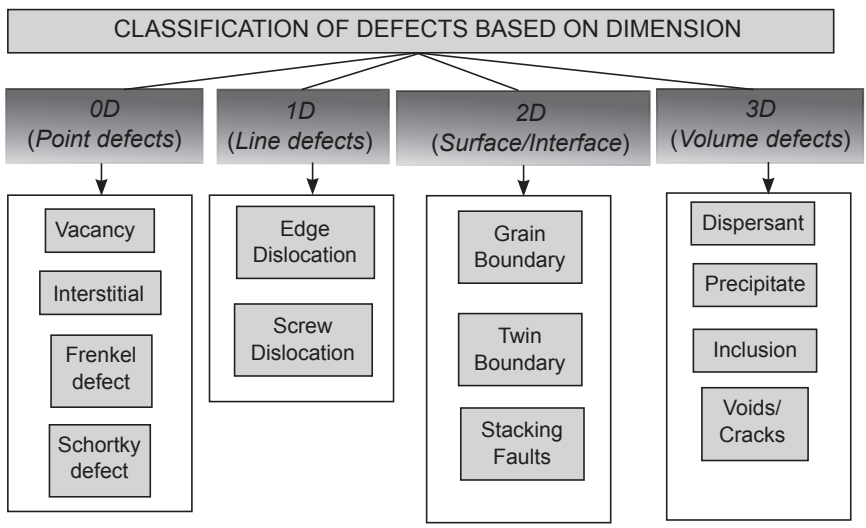


Fig. 1.8 Defects based on Dimensions

Point defects Point defects are simple to visualize and they play crucial roles in impurity diffusion. In layman language anything other than a silicon atom on a lattice site constitute a point defect. By this definition a substitutional doping atom is a point defect and might be referred to as an impurity related defect. Principally point defect can be further divided in two categories: the first is simply missing silicon lattice atom or vacancy and the other is an extra silicon atom.

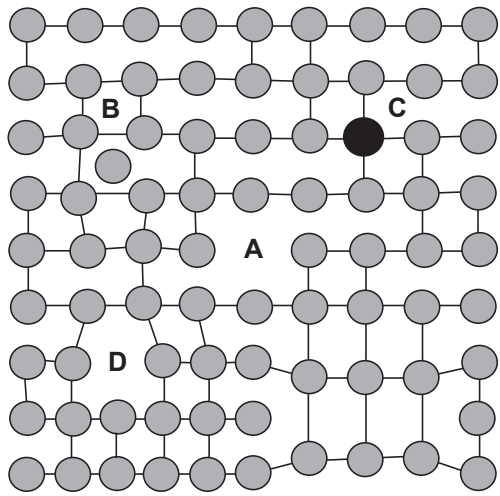


Fig. 1.9 Simple semiconductor defects A-vacancies, B- interstitials, C- substitutional impurities, D- edge dislocation

Point defect include vacancies, interstitials, misplaced atoms, dopant impurity atoms deliberately introduced for the purpose of controlling the electronic properties of the semiconductor and impurity atoms which are used as contaminations during material growth or processing. Figure 1.9 shows different types of point defects in the crystal lattice.

One of the most common types of point defect is a lattice site without an atom. This defect is a vacancy figure 1.9A. Closely related point defect is an atom that resides not on a lattice site, but the spaces between the adjacent lattice positions. It is referred to as an interstitial figure 1.9B. If the interstitial or vacancy atom is of the same material as the atoms in the lattice; it is a self-interstitial. In some cases, the interstitial comes from a nearby vacancy such a vacancy interstitial combination is called a Frenkel defect. The interstitial or vacancy may not remain at the site at which it was created. Both types of defects can move through the crystal particularly under the high temperature ambience that arises during processing condition. Either defect might also migrate to the surface of the wafer where it is annihilated.

The second type of point defect that may exist in a semiconductor is known as extrinsic defect shown in figure 1.9C. This is caused either by an impurity atom at an interstitial site or at a lattice site. In the second case it is referred to as a *substitution impurity*. For example dopant atoms are required to modulate semiconductor conductivity are basically caused by substitutional defects. Substitutional as well as interstitial impurities have a significant impact on device performance. Some impurities that tend to occupy interstitial sites have electronic states near the center of the bandgap. As a result, they are efficient sites for the recombination of electron-hole pair. These recombination centers form depletion region that reduce the gain of bipolar transistors and can cause p–n diodes to leak.

Line Defects: Line defects or dislocations, are lines along which whole rows or columns of atoms in a solid crystal are arranged anomalously. The resulting irregularity in spacing is most severe along a line called the line of dislocation as shown in figure 1.10. Line defects are mostly due to misalignment of ions or presence of vacancies along a line that can be weaken or strengthen solids. When lines of ions are missing in an otherwise perfect array of ions, an edge dislocation appeared which is responsible for the ductility and malleability. In fact movement of edge dislocation often results hammering and stretching of materials. Movements of dislocations give rise to their plastic behavior. Line dislocations usually do not end inside the crystal, they form loops or end at the surface of a single crystal.

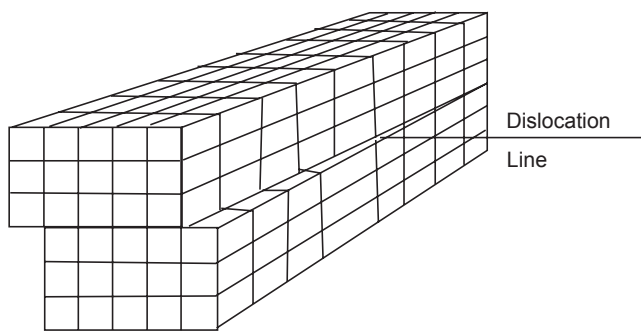


Fig. 1.10 Line dislocation

A dislocation is characterized by the term known as Burgers vector; If you will imagine going around the dislocation line, and exactly going back as many atoms present in each direction as one have gone forward, one will not come back to the same atom where he has started. The Burgers vector points from start atom to the end atom of this journey and this "journey" is known as Burgers circuit in line dislocation theory.

Figure 1.11 shows the Burger circuit journey around an edge dislocation using the sketch of surface of a crystal. A Burger vector is approximately perpendicular to the dislocation line, and the missing line of atoms is somewhere within the block of the Burger journey.

If the misalignment shifts a block of ions gradually downwards or upwards causing the formation of a screw like deformation, a screw dislocation is formed as shown in figure 1.11(b).

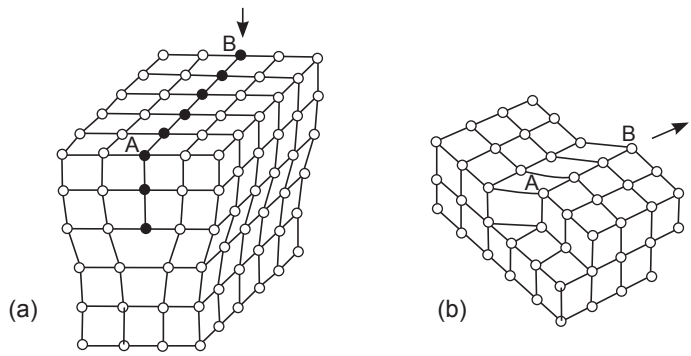


Fig. 1.11 (a) Edge dislocation formation in crystal and (b) screw dislocation formation in crystals

Line defect affects the mechanical properties of the solid in terms of its density as well as deteriorates the structure along a one-dimensional space. Mechanical properties are also affected by the type of line defects. As a result for structural materials, the formation and study of dislocations are particularly important.

Surface Defects: These defects may arise at the boundary between two grains, or merging of two crystals such as small crystal within a larger crystal. The rows of atoms in two different grains may run in slightly different directions, leading to a mismatch across the grain boundary as shown in figure 1.12. The external surface of a crystal also comes under surface defect because the atoms on the surface relocate their positions to accommodate for the absence of neighboring atoms.

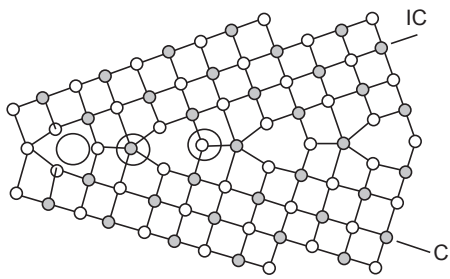


Fig. 1.12 Surface defects

Volume or Bulk Defects

Volume or bulk defects are 3-dimensional defects. These include cracks, pores, external inclusions and several other phases. These defects are generally introduced during fabrication steps. All these defects are capable of acting as stress raisers therefore harmful to parent material's mechanical behavior. However, in some cases foreign particles are added selectively and purposefully to mechanically strengthen the material. The procedure in which foreign particles act as obstacles to movement of dislocations, which facilitates plastic deformation is known as dispersion hardening. The second-phase particles act in two different ways – first particles are either may be cut by the dislocations and secondly the particles resist cutting and dislocations are forced to bypass them. Due to ordered particles strengthening is responsible for the good high-temperature strength on many alloys. However, pores are harmful because they reduce effective load bearing area and act as stress concentration sites.

It is common to divide aggregates of atoms or vacancies into four classes in an imprecise classification that is based on a combination of the size and effect of the particle. The four categories are: (A) **Precipitates**, which area fraction of a micrometer in size and decorate the crystal; (B) **Dispersants** or second phase particles, which vary in size from a fraction of a micrometer to the normal grain size (10-100μm), but are intentionally introduced into the microstructure; (C) **Inclusions**, which vary in size from a few microns to macroscopic dimensions, and are relatively large, undesirable particles that entered the system as dirt or formed by precipitation; (4) **Voids or pores**, which are holes in the solid formed by trapped gases or by the accumulation of vacancies.

Precipitates are small particles that are introduced into the matrix by solid state reactions. The precipitates are used for several purposes, their most useful purpose is to increase the strength of structural alloys by acting as hurdles to the motion of dislocations. Their efficiency in doing this depends on several factors such as their internal properties, their size, and their distribution throughout the lattice. However, their role in the microstructure is to modify the behavior of the crystal matrix rather than to act as separate phases in their own right.

Dispersants are bigger particles that behave as a second phase and influence the behavior of the primary phase. They may be large precipitates, grains, or polygranular particles distributed through the microstructure.

Inclusions are foreign particles or large precipitate particles. They are usually unwanted constituents in the microstructure. Inclusions have a harmful effect on the strength of structural alloys since they are preferential sites for failure.

They are most time harmful in microelectronic devices as they change the geometry of the device by interfering in fabrication, or alter its electrical properties by hosting undesirable properties of their own.

Voids are produced as a result of gases those are trapped during solidification or by vacancy condensation in the solid state. So they are almost always undesirable defects. Their prime effect is to decrease mechanical strength and endorse fracture at small loads.

1.7 SI PROPERTIES & ITS PURIFICATION

More than 90% of earth crust is composed of Silica (SiO_2) or Silicate making Si the second most abundant element on earth after oxygen. It is found in rocks, sand, clays and soils combined with oxygen as SiO_2 or silicates. Si is the fourteen element of the periodic table and is a group IVA element. Pure Si is a dark gray solid with the same crystalline structure as diamond; with each atom covalently bonded to four nearest neighbors. In pure form its lattice constant is 5.43086 Å at 300K. The nearest neighbor distance between Si atom in diamond lattice is 2.35163 Å. Si has a melting point of 2570°F (1410°C), a boiling point of 4271°F (2355°C) and a density of 2.33 g/cm^3.

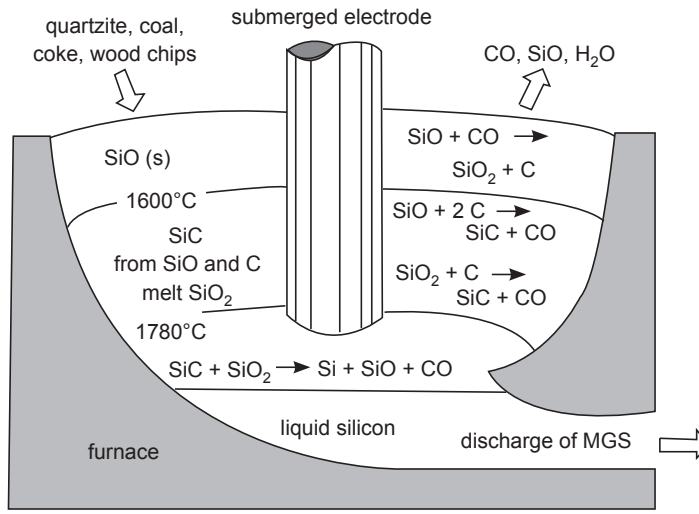


Fig. 1.13 Formation of MGS through arc furnace

The Si industry depends on a ready supply of inexpensive high quality single crystal wafer. IC manufactures typically specify physical parameter (diameter, thickness, flatness, mechanical defect etc.) electrical parameters (N or P type, dopant, resistivity etc.) and finally impurity levels (oxygen and carbon in particular) when purchasing wafers. For single crystalline Si wafer, Si must be refines as well as be converted into crystalline form. This is usually a

multistage process beginning with sand (SiO_2) name as Quartzite. Conversion the quartzite to Metallurgical Grade Silicon (MGS) is the initial step in refining process. Figure 1.13 shows the production of MGS from arc furnace. This process usually takes place in a furnace in which the quartzite and carbon source (coal or coke) mixture is heated to temperature approaching 2000°C.

$$2C\ (s) + SiO_2\ (s) = Si\ (l) + 2CO\ (g)$$

The MGS grade Si that results is about 98% pure, with Al and iron being two of the dominant impurities most of MGS is used in manufacturing Al or Silicon Polymers.

To convert the MGS into highly purified polycrystalline Electronic Graded Silicon (EGS) multi stage process is required. Pure EGS generally requires that the doping elements reduced to be in ppm range and carbon impurities should be less than 2 ppm. In MGS major impurities are boron, carbon and residual donors. Seimens Process is one of the major techniques for converting MGS to EGS. The numbers of steps to convert MGS to EGS are: first step MGS reacts with gaseous HCl, commonly by grinding the MGS into a fine powder and then the reaction takes place in the presence of catalyst at elevated temperature. This process can form any number of Si-H-Cl compounds (SiH_4→ silane; SiH_3Cl→chlorosilane; SiH_2Cl_2→ dichlorosilane; $SiHCl_3$→ trichlorosilane or $SiCl_4$→silicon tetra chloride)

$$Si\ (s) + 3HCl\ (g) \longrightarrow SiHCl_3\ (g) + H_2\ (g) + Heat$$

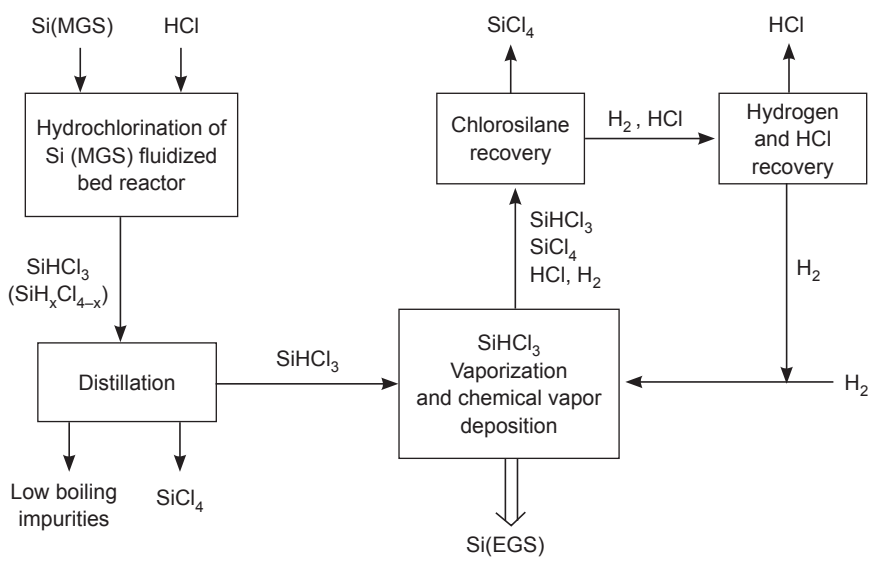


Fig. 1.14 Conversion steps of MGS to EGS