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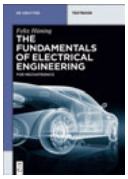

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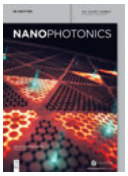

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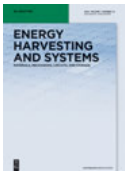

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Nano Devices and Sensors

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ISBN 978-1-5015-1050-2
e-ISBN (PDF) 978-1-5015-0153-1
e-ISBN (EPUB) 978-1-5015-0155-5
Set-ISBN 978-1-5015-0154-8

Library of Congress Cataloging-in-Publication Data
A CIP catalog record for this book has been applied for at the Library of Congress.

Bibliographic information published by the Deutsche Nationalbibliothek
The Deutsche Nationalbibliothek lists this publication in the Deutsche Nationalbibliografie; detailed bibliographic data are available on the Internet at http://dnb.dnb.de.

Cover image: Petrovich9/Signature Collection/istock by Getty Images
Typesetting: Lumina Datamatics
Printing and binding: CPI Books GmbH, Leck
© Printed on acid-free paper
Printed in Germany

www.degruyter.com

Editorial/Foreword

The chapters in this edited book are written by some authors who have presented very high quality papers at the 2015 International Symposium of Next-Generation Electronics (ISNE 2015) held in Taipei, Taiwan. The ISNE 2015 was intended to provide a common forum for researchers, scientists, engineers, and practitioners throughout the world to present their latest research findings, ideas, developments, and applications in the general areas of electron devices, integrated circuits, and microelectronic systems and technologies. The scope of the conference includes the following topics:

A. Green Electronics
B. Microelectronic Circuits and Systems
C. Integrated Circuits and Packaging Technologies
D. Computer and Communication Engineering
E. Electron Devices
F. Optoelectronic and Semiconductor Technologies.

The technical program consisted of 4 plenary talks, 23 invited talks, and more than 250 contributed oral and poster presentations. Plenary speakers were recognized experts in their fields, and their talks focused on leading-edge technologies including:

"The Future Lithographic Technology for Semiconductor Fabrication," by Dr. Alek C. Chen, Asia ASML, Taiwan.

"Detection of Single Traps and Characterization of Individual Traps: Beginning of Atomistic Reliability Physics," by Prof. Toshiaki Tsuchiya, Shimane University, Japan.

"The Art and Science of Packaging High-Coupling Photonics Devices and Modules," by Prof. Wood-Hi Cheng, National Chung-Hsing University, Taiwan.

"Prospect and Outlook of Electrostatic Discharge (ESD) Protection in Emerging Technologies," by Prof. Juin J. Liou, University of Central Florida, USA.

After a rigorous review process, the ISNE 2015 technical program committee has selected 10 outstanding presentations and invited the authors to prepare extended chapters for inclusion in this edited book. Of the 10 chapters, five are focused on the subject of electronic devices, and the others cover the circuit designs for various applications. The authors are working at the academia in Austria, United States, Korea, and Taiwan.

The guest editors would like to take this opportunity to express our sincere gratitude to all the members of the ISNE 2015 technical program committees for reviewing the papers and selecting the manuscripts for the edited book. We also thank all the authors for their valuable and excellent contributions to the book.

Guest Editors:

Juin J. Liou *University of Central Florida, USA*
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Contents

Chunsheng Jiang, Renrong Liang, Jing Wang, and Jun Xu

Subthreshold Behaviors of Nanoscale Silicon and Germanium Junctionless Cylindrical Surrounding-Gate MOSFETs

Abstract: When the traditional planar metal-oxide-semiconductor-field-effect transistors (MOSFETs) encounter insurmountable bottleneck of static power dissipation, junctionless transistor (JLT) becomes a promising candidate for sub-22 nm nanoscale devices due to its simpler fabrication process and better short-channel performances. Subthreshold behaviors dominate the standby power of nanoscale JLTs. In this chapter, a physics-based analytical model of electrostatic potential for both silicon and germanium short-channel junctionless cylindrical surrounding-gate (JLCSG) MOSFETs operated in the subthreshold regime is proposed, in which the full two-dimensional (2D) Poisson's equation is solved in the channel region by a method of series expansion. The expression of the proposed electrostatic potential is completely rigorous and explicit. Based on this result, the expressions of threshold voltage, subthreshold drain current, and subthreshold swing for JLCSG MOSFETs are derived. Subthreshold behaviors are studied in detail by changing different device parameters and bias conditions, including doping concentration, channel radius, gate length, gate equivalent oxide layer thickness, drain voltage, and gate voltage. Results predicted by all the analytical models agree well with numerical solutions from the three-dimensional simulator. These analytical models can be used to investigate the operating mechanisms of nanoscale JLCSG MOSFETs and to optimize their device performances.

Keywords: Junctionless transistor, analytical model, germanium devices, short-channel effects, subthreshold behaviors, surrounding-gate devices.

1 Introduction

Planar metal-oxide-semiconductor-field-effect transistor (MOSFET) has been the workhorse of integrated circuit industry since it was born in 1960 [1]. Performances for planar MOSFETs have been steadily improved due to the scaling down law, which is famous as Moore's law [2]. However, as the gate length of MOSFET scales into sub-22

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nm node, the standby power challenge due to the subthreshold leakage current and the gate tunneling leakage current has become a primary roadblock for low-power applications. The gate tunneling leakage current could be remarkably removed by high-k/metal gate technology [3]. The increase in subthreshold leakage current is mainly caused by the short-channel effects (SCEs), mostly including the threshold voltage roll-off, drain-inducing barrier lowering (DIBL) effect and transverse velocity saturation effect. SCEs result from sharing control over the channel among the source region, drain region, and gate electrode. Multigate transistors, such as double-gate MOSFET, triple-gate MOSFET, Ω–gate MOSFET, ∏–gate MOSFET, and surrounding-gate MOSFET, have been proposed to suppress the SCEs by encircling the device channel and the gate controllability could be boosted [4]. Meanwhile, it's another serious challenge for semiconductor manufacture process to produce ultra-sharp source/drain junctions in the range of several nanometers for the nanoscale transistors. Junctionless transistor (JLT) has been proposed to solve this problem [5]. The JLT is basically a gated resistor where the source region, drain region, and channel region have the same dopant type and concentration without any junctions between them.

The advantages of JLTs compared with its inversion-mode MOSFET counterpart are that: (1) it drastically simplifies the fabrication process; (2) it eliminates the lateral impurity diffusion and solves the problem of sharp doping profile formation; (3) it was demonstrated that the short-channel performances, such as DIBL effect and subthreshold slope degradation, were improved when the device sizes were aggressively scaled down [6]; (4) the mobility degradation in the high electric field region is relaxed [7]; (5) the gate dielectric thickness scaling is also relaxed in terms of the intrinsic delay time [5]. Nevertheless, it requires the full depleted channel when JLT works at the off-state in order to turn the device off completely. This is very difficult for the planar structure owing to its weak gate controllability. Thus, multigate structures or three-dimensional (3D) structures can be a good choice to suppress the subthreshold leakage current for JLTs. In practice, almost all of the experimental verifications for JLT concept adopt 3D architectures [8–11]. Another method is replacing the silicon-on-insulator (SOI) substrate with bulk substrate [12]. This method is ideal because the subthreshold leakage current depends on the effective channel layer thickness. In a bulk substrate structure, the effective channel layer thickness can be less than the physical thickness due to the depletion-layer width of p–n junction between the channel and substrate (well) with controllable well doping concentration and/or well bias. Theoretically, the surrounding-gate configuration has the best short-channel performances [13]. As a consequence, junctionless cylindrical surrounding-gate (JLCSG) transistor becomes one of the promising candidates for next-generation digital switch device.

In addition, germanium (Ge) has been considered as one of the promising channel materials in replacement of silicon (Si) for future high-speed CMOS technology because of its high electron mobility (3,900 cm^2/Vs), hole mobility (1,900

cm^2/Vs), and best Si compatibility. Ge has been widely investigated in recent years [14–16]. Generally speaking, Ge p-MOSFETs have better performances, whereas Ge n-MOSFETs have exhibited poor drive current and inversion mobility, lower than universal Si mobility, as reported by several different research groups worldwide due to the difficulties in the surface passivation and n-type dopant activation [17–20]. As a result, Ge complementary metal-oxide-semiconductor transistor (CMOS) structure is difficult to be achieved. However, recently, Shoichi Kabuyanagi group [21] demonstrated the high electron mobility in Ge n-channel junctionless FETs compared with Si n-channel MOSFETs. This phenomenon is the resultant effect of the bulk conduction mechanism of junctionless transistors and material properties of Ge. As a result, Ge n-channel JLCSG MOSFET is noteworthy. In this chapter, an analytical short-channel electrostatic model was proposed for Si and Ge JLCSG MOSFETs and their subthreshold behaviors were studied extensively by both proposed analytical model and a 3D commercial numerical simulator [22]. The modeled data are in good agreement with simulated data.

2 Silicon junctionless cylindrical surrounding-gate transistors

Si material dominates the present semiconductor manufacturing industry and has best mature fabrication technology because of its good properties and very low cost. Therefore, Si-based JLTs should be studied first. In fact, almost all of the experimental reports on JLTs are based on Si material [23–25].

2.1 The working principle for JLCSG transistor

JLT is a kind of intrinsic depletion mode device contrary to the traditional inversion-mode MOSFET. Figure 1(a) shows the landscape of an n-type JLCSG MOSFET. Figure 1(b) presents the corresponding cross-sectional schematic diagram along channel direction and coordinates. At zero-gate voltage, a high workfunction (WF) difference between the gate metal and channel material has to be achieved to deplete the entire channel of JLCSG transistors with a suitable threshold voltage value. The operation regimes can be generally classified as full depleted region, partly depleted region, flat-band channel region, and accumulation region [26]. Figure 2 presents the responding energy band diagrams for the four operation regimes. V_{th} is the long-channel threshold voltage for the n-type JLCSG transistor [27].

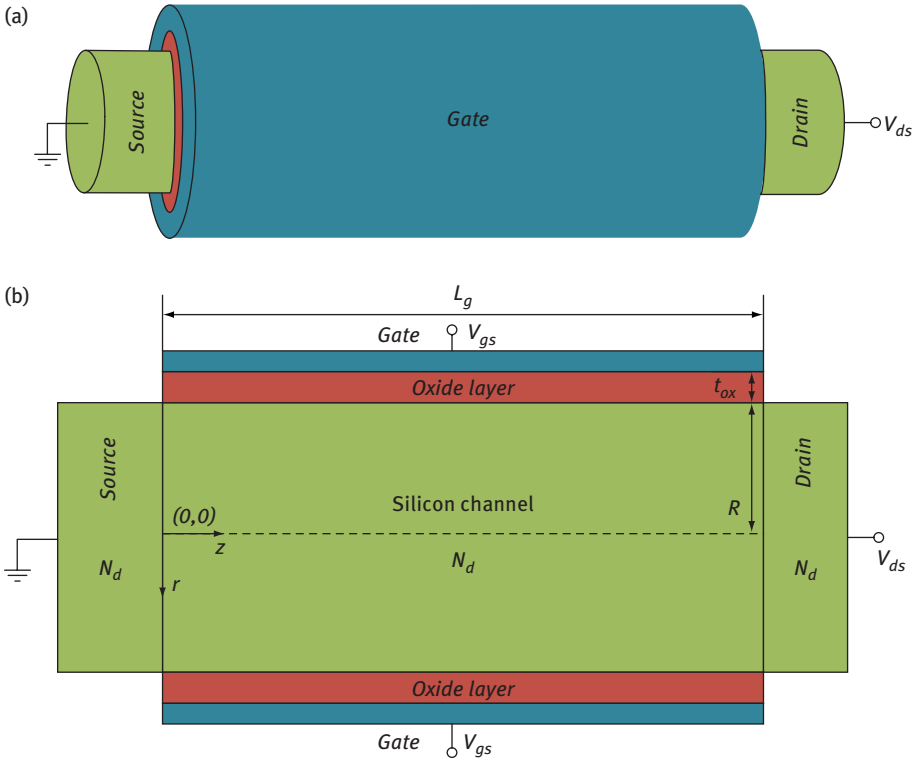

Fig. 1: (a) The landscape of an n-type Si JLCSG MOSFET; (b) cross-sectional schematic diagram along channel direction and coordinates of the device.

$$V_{TH} = V_{FB} - \frac{qN_dR^2}{4\varepsilon_{si}} - \frac{qN_dR}{2C_{ox}} \tag{1}$$

and

$$V_{FB} = (\varphi_m - \varkappa - \frac{E_g}{2})/q + v_t \ln(\frac{N_d}{n_i}) \tag{2}$$

where V_{FB} is the flat band voltage; q is the electronic charge; N_d is the doping concentration of the channel; R is the radius of the channel; ε_{si} is the dielectric constant of Si; C_{ox} is the capacitance per unit area of the gate dielectric, $C_{ox} = \varepsilon_{ox}/[Rln(1 + t_{ox}/R)]$;[28] ε_{ox} is the permittivity of the oxide layer; t_{ox} is the equivalent oxide layer thickness, defined as $(\varepsilon_{ox}t_{high-k})/\varepsilon_{high-k}$, t_{high-k}, ε_{high-k} are the thickness and permittivity of the high-k gate dielectric materials, respectively [29]. φ_m is the workfunction of the gate metal. $\varkappa$ is the electron affinity of Si. E_g is the band gap of Si. n_i is the intrinsic carrier concentration of Si. v_t is the thermal voltage, defined as kT/q. It can be observed

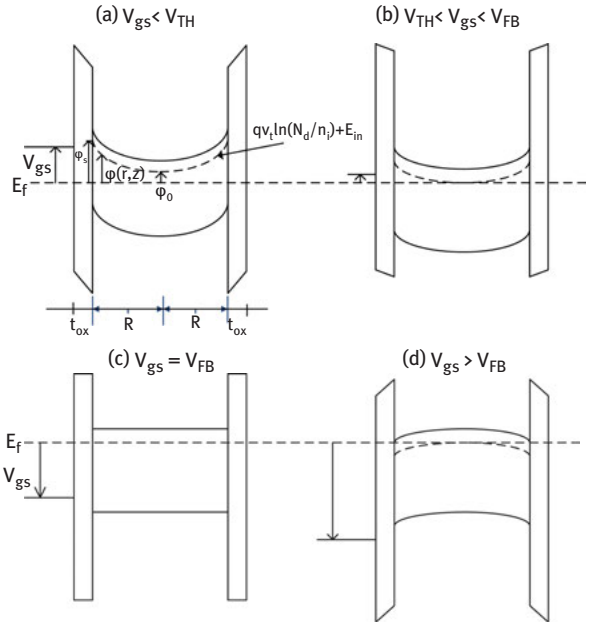

Fig. 2: The energy band diagrams for a n-type JLCSG transistor (a) full depleted region; (b) partly depleted region; (c) flat band region; (d) accumulation region. The potential $\varphi(r,z)$ is defined as the sum of intrinsic Si midgap level (E_{in}) and $qv_t ln(N_d/n_i)$ referenced to the Fermi level (E_f).

from Eqn. (1) that design parameters: R, t_{ox}, N_d, and φ_m must be optimized to achieve better subthreshold performances because the subthreshold leakage current is very sensitive to V_{th}. Eqn. (1) also indicates the biggest shortcoming of JLTs for digital logic application: the performances depend strongly on the geometry (R, t_{ox}, and L_g) as well as on the doping level of the channel (N_d) and the process variation is bigger than that of junction-based MOSFETs. However, these parameters can be used to finely tune the operation point of the device, which makes the application of JLTs in low-power sensing systems very promising [30].

It is noteworthy that V_{th} can be a positive value for the normally off device and be a negative value for the normally on device by adjusting device parameters. Thus, JLTs can satisfy the requirement of multithreshold electronics system easily, which has emerged as a promising technique to reduce leakage power dissipation and boot high performances at the same time [31].

2.2 Short-channel effects (SCEs) and subthreshold behavior model

SCEs are very important nonideal secondary effects, mainly including threshold voltage roll-off, DIBL effect, and transverse velocity saturation effect, and so on.

SCEs dominate the subthreshold leakage current, which is the most important component of static power dissipation. For nanoscale JLCSG MOSFETs, analytical models are urgently needed to guide the device design and circuit simulation. However, most studies have concentrated on long-channel models of JLCSG MOSFETs [27, 28, 32, 33], in which the one-dimensional (1D) Poisson's equation is solved based on the gradual channel approximation (GCA). These models are not suitable for short-channel JLCSG MOSFETs, where two-dimensional (2D) effects play a key role. A few studies have been reported that investigate the subthreshold behaviors of JLCSG MOSFETs, in which the quasi 2D Poisson's equation is solved based on the parabolic-profile approximation (PPA) [34–36]. However, PPA is a purely conceptual hypothesis and lacks real physical meaning. For a cylindrical surrounding-gate structure, the conventional separation of variables for series solution to 2D Poisson's equation will introduce a transcendental equation of eigenvalues, which can only be solved numerically [37].

In next sections, a method of series expansion [38, 39] is applied to determine the analytical solutions of the 2D Poisson's equation of JLCSG MOSFETs. This method can avoid the difficulties described above. Thus, the proposed 2D electrostatic potential model is completely rigorous and explicit. Using this model, analytical models for the metrics such as threshold voltage, subthreshold drain current, and subthreshold swing are derived to depict the subthreshold characteristics. The accuracy of all the developed analytical models is verified by numerical simulation using a 3D commercial device simulator.

2.3 An analytical model for Si short-channel junctionless cylindrical surrounding-gate MOSFETs

2.3.1 Electrostatic potential model

As shown in Figure 1(b), because the doping concentration is very high in the source and drain regions, the voltage drop across these two regions can be ignored. In the subthreshold regime, mobile carriers can be ignored [35]. Furthermore, it is presumed that the channel is fully depleted because of an ultra-small channel radius. For a uniform doped body, Poisson's equation for channel region is

$$\frac{\partial^2 \varphi}{\partial r^2} + \frac{1}{r}\frac{\partial \varphi}{\partial r} + \frac{\partial^2 \varphi}{\partial z^2} = -\frac{qN_d}{\varepsilon_{si}} \tag{3}$$

where $-R \le r \le R$ and $0 \le z \le L_g$. R is the radius of the channel; L_g is the gate length. φ is the electrostatic potential.

From refs. [38, 39], φ can be written as

$$\varphi(r,z) = V_{ref} + \frac{V_{ds}}{L_g}z + \sqrt{\frac{2}{L_g}}\sum_{n=1}^{\infty} A_n(r) sin\frac{n\pi}{L_g}z \tag{4}$$

where V_{ref} is the electrostatic potential of the source region relative to the cathode of the power supply. V_{ds} is the drain voltage. In this work, V_{ref} is 0.53 V at room temperature.

Substitute Eqn. (4) into (3), $A_n(r)$ is an auxiliary parameter and satisfies equation:

$$\frac{d^2A_n(r)}{dr^2} + \frac{1}{r}\frac{dA_n(r)}{dr} - \lambda_n^2 A_n(r) = f_n \tag{5}$$

where

$$\lambda_n = \frac{n\pi}{L_g} \tag{6}$$

and

$$f_n = -\frac{qN_d}{\varepsilon_{si}\lambda_n}\sqrt{\frac{2}{L_g}}[1-(-1)^n] \tag{7}$$

The general solution of Eqn. (5) is

$$A_n(r) = c_n I_0(\lambda_n r) + d_n K_0(\lambda_n r) - \frac{f_n}{\lambda_n^2} \tag{8}$$

where $I_0(x)$ is the zero-order first kind of imaginary Bessel function, and $K_0(x)$ is the zero-order second kind of imaginary Bessel function. Coefficients, c_n and d_n are defined by following boundary conditions:

$$\varphi(r,0) = V_{ref} \tag{9}$$

$$\varphi(r,L) = V_{ds} + V_{ref} \tag{10}$$

$$\frac{\partial\varphi}{\partial r}|_{r=0} = 0 \tag{11}$$

$$C_{ox}[V_{gs} - V_{FB} - \varphi(R,z)] = \varepsilon_{si}\frac{\partial\varphi}{\partial r}|_{r=R} \tag{12}$$

Eqns. (9) and (10) denote boundary conditions at the source and drain regions, respectively. It is easy to be verified that Eqn. (4) satisfies the boundary conditions of Eqns. (9) and (10) automatically. Eqn. (11) is valid because of the symmetry of the device. Eqn. (12) is derived from Gauss's theorem at the interface of the gate dielectric layer and silicon channel. From Eqns. (8)–(12), we get

$$d_n = 0 \tag{13}$$

$$c_n = \left[\frac{f_n}{\lambda_n^2} + \sqrt{\frac{2}{L_g}}\frac{L_g}{n\pi}(-1)^n(V_{ds} + V_{FB} - V_{gs}) - \sqrt{\frac{2}{L_g}}\frac{L_g}{n\pi}(V_{FB} - V_{gs})\right] \Big/ \left[\frac{\varepsilon_{si}}{C_{ox}}\lambda_n I_1(\lambda_n R) + I_0(\lambda_n R)\right] \tag{14}$$

where $I_1(x)$ is the first-order first kind of imaginary Bessel function. At last, we obtain the expression electrostatic potential:

$$\varphi(r,z) = V_{ref} + \frac{V_{ds}}{L_g}z + \sqrt{\frac{2}{L_g}}\sum_{n=1}^{\infty}\left[c_n I_0(\lambda_n r) - \frac{f_n}{\lambda_n^2}\right]\sin\frac{n\pi}{L_g}z \tag{15}$$

where c_n is given by Eqn. (14). To verify the accuracy of the developed models, the results of analytical models were compared with those of a 3D numerical simulation tool. There are few mobile carriers in the channel when the JLCSG device is operated in the subthreshold regime. Quantum effects can be ignored when $R \geq 5$ nm in the developed models and simulation [36]. For both analytical calculation and simulation, a dopant-dependence mobility model: Masetti model [40] is used. The device temperature is 300 K, and the workfunction of the gate metal is 4.8 eV.

It should be noted that the Eqn. (15) is an infinite series and we have to used first several terms to approximate $\varphi(r,z)$. The convergence of A_n should be tested firstly. Actually, A_n converges very quickly with respect to argument n, as presented in Figure 3. It can be observed that high-order terms $(n \geq 4)$ are far less than the first three terms. As the gate length increases, the error due to high-order terms increases. This fact indicates that our model is more suitable for short-channel devices $(10\,\text{nm} \leq L_g \leq 40\,\text{nm})$. Even though, the first three order approximations have enough precision to calculate the model expressions for any given gate length and channel radius and the first three order approximations are employed to compute the electrostatic potential, subthreshold drain current and subthreshold swing, only the first order term is considered in the threshold voltage model for simplification.

Figure 4 illustrates the central electrostatic potential along channel direction for different gate lengths. The modeled data match well with simulated data. It can be seen that as the gate length decreases, the position of the minimum central potential is pulled up and leading to a lower threshold voltage. This phenomenon is called the threshold voltage roll-off [41] and deteriorates the device subthreshold performances.

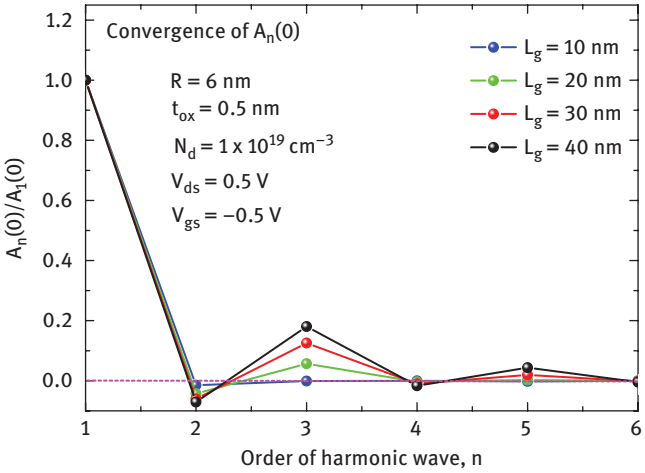

Fig. 3: Ratio of $A_n(0)/A_1(0)$, showing the convergence of coefficient, $A_n(0)$. Higher order terms ($n \geq 4$) are far less than the first three terms.

Figure 5 presents the electrostatic potential distribution in the channel center as a function of channel radius. Analytical results for the proposed model are in good agreement with the 3D simulation results. It is clear that, as the channel radius increases, the minimum central potential along the channel direction is elevated, which suggests that the gate gradually loses control over the channel. This fact leads to a smaller threshold voltage for a larger channel radius, degrading the subthreshold characteristics. Hence, a smaller channel radius is desired to reduce the leakage current.

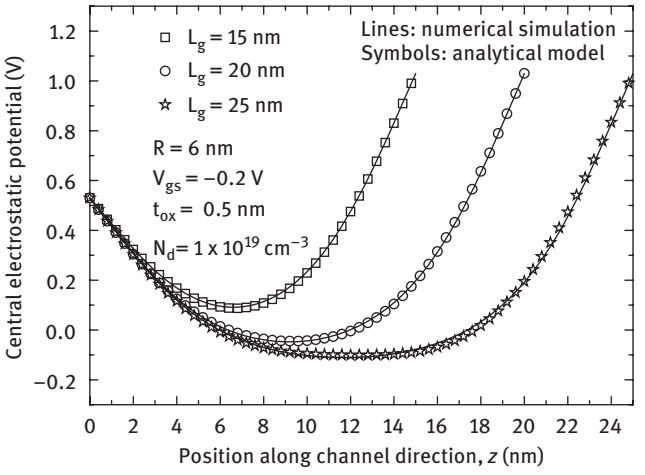

Fig. 4: Central electrostatic potential along channel direction for different gate lengths. The simulated device parameters are $V_{gs} = -0.2$ *V*, $R = 6$ nm, $V_{ds} = 0.5$ *V*, $N_d = 1 \times 10^{19}$ cm^{-3}, and $t_{ox} = 0.5$ nm.

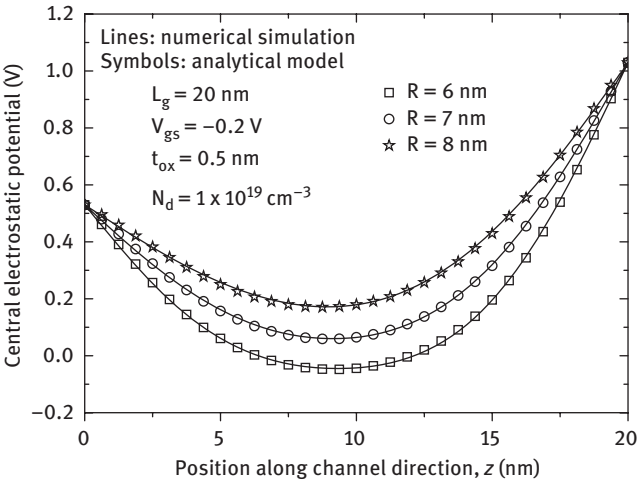

Fig. 5: Central electrostatic potential along channel direction for different radiuses. The simulated device parameters are L_g = 20 nm, V_{gs} = −0.2 *V*, V_{ds} = 0.5 *V*, t_{ox} = 0.5 nm, and N_d = 1 × 10^{19} cm^{-3}.

It is shown in Figure 6 that the central electrostatic potential distribution for different equivalent oxide layer thicknesses, t_{ox}. It is clear that, as the equivalent oxide layer thicknesses steadily increases, the position of the minimum central potential is pulled up, which shows that the gate electrode gradually loses control of the channel. This is because a thicker equivalent oxide layer will resist the vertical electric field from the metal gate penetrating into the channel, resulting in the degradation of threshold behaviors. Therefore, to suppress the SCEs, thin equivalent oxide thickness is preferred.

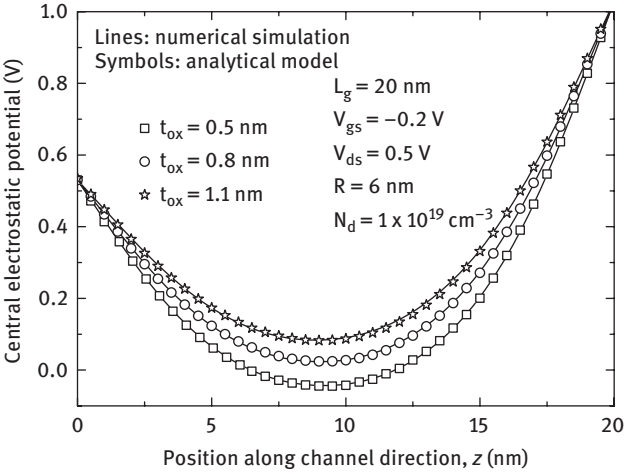

Fig. 6: Central electrostatic potential distribution along channel direction for different equivalent oxide layer thicknesses. The simulated device parameters are L_g = 20 nm, V_{gs} = −0.2 *V*, V_{ds} = 0.5 *V*, *R* = 6 nm, and N_d = 1 × 10^{19} cm^{-3}.

It is observed in Figure 7 that the central electrostatic potential distribution for different drain voltages. It is obvious that, as V_{ds} steadily increases, the position of the minimum central potential is raised, which shows that the channel can be turned on more easily. The phenomenon is called drain inducing barrier lowering (DIBL) effect [42].This is a kind of important SCEs.

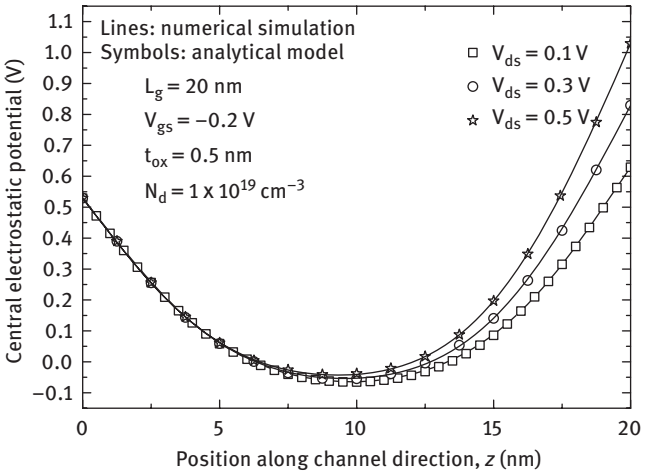

Fig. 7: Central electrostatic potential along channel direction for different drain voltages. The simulated device parameters are L_g = 20 nm, V_{gs} = −0.2 *V*, R = 6 nm, and N_d = 1 × 10^{19} cm^{-3}.

Figure 8 shows the electrostatic potential at r = 0 nm along the channel direction for different gate voltages. The center electrostatic potential is proportional to V_{gs} because of the capacitive coupling effect between the gate dielectric-layer capacitance and channel capacitance. The analytical model curves match well with the simulated curves for a wide range of gate voltages, even for devices with a short gate length (L_g = 20 nm), which indicates the validity of the developed model for calculating the potential profile.

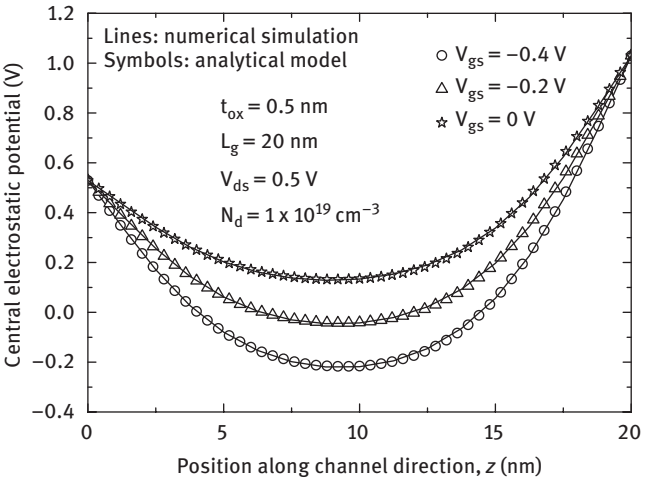

Fig. 8: Central electrostatic potential along channel direction for different gate voltages. The simulated device parameters are L_g = 20 nm, V_{ds} = 0.5 *V*, R = 6 nm, and N_d = 1 × 10^{19} cm^{-3}.

2.3.2 Threshold voltage model

Figure 9 presents the 2D electrostatic potential contours of channel cut plane along z direction. The data are calculated from numerical simulation. It can be observed that along z direction, there exists a minimum potential position ($z = z_o$) for given position r. Different points along z direction can be treated as many switches in a series. So, the minimum potential position along z direction will switch on at last and determines the onset of conduction. On the other hand, there exists a maximum potential position along r direction for given position z. Different points along r direction can be treated as many switch in parallel, so the maximum potential position will switch on at first and also determines the onset of conduction. Above all, because of the device symmetry, the position (0, z_o) will conduct current firstly and determines the subthreshold behaviors of JLCSG MOSFETs. The position (0, z_o) is called the most leaky path or the virtual electrode [43, 44]. Similar to the definition of long channel threshold voltage, the short-channel threshold voltage, $V_{ths,}$ is defined as the gate voltage when $\varphi(0, z_0)$ reaches V_{ref} $-2kT/q$; in this situation, the electron density at the virtual electrode is $N_d exp(-2)$. This value is far less than N_d. Therefore, the mobile electrons in the channel can be ignored. Such a definition is equivalent to the constant drain current method of V_{th} extraction [35].

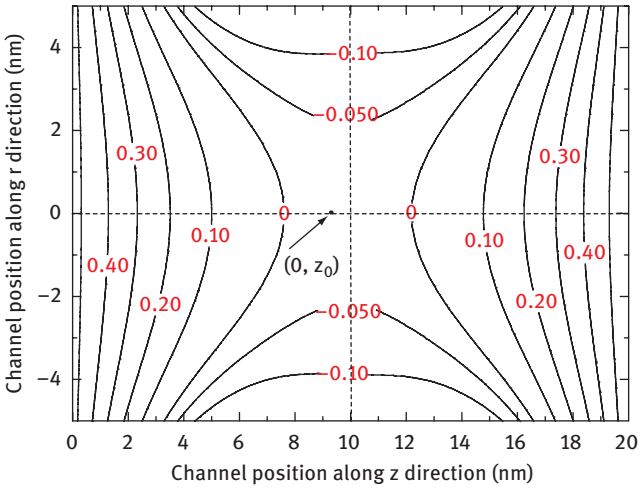

Fig. 9: The 2D electrostatic potential contours of channel cut plane along z direction. The data are calculated from numerical simulation. The simulated device parameters are L_g = 20 nm, t_{ox} = 2 nm, R = 5 nm, V_{gs} = −1 V, and V_{ds} = 0.05 V.

$$\varphi(0, z_0) = V_{ref} + \frac{V_{ds}}{L_g} z_0 + \sqrt{\frac{2}{L_g}} \sum_{n=1}^{\infty} \left[c_n - \frac{f_n}{r_n^2} \right] \sin \frac{n\pi}{L_g} z_0 \tag{16}$$

z_0 can be found by letting

$$\frac{\partial \varphi(0, z)}{\partial z}|_{z=z_0} = 0 \tag{17}$$

For a long-channel device, only the first-order term is considered and z_0 can be approximated as

$$z_0 = \frac{L_g}{\pi} \arccos\left(\frac{V_{ds}}{2[2(V_{FB} - V_{gs}) + V_{ds}]} \right) \tag{18}$$

From Eqn. (18), it can be observed that z_0 is equal to $L_g/2$ for V_{ds} = 0 V. When $V_{ds} \neq 0V$, the position of the minimum potential is slightly closer to the source region, slightly less than $L_g/2$. The value of z_0 is calculated to be $0.4L_g - 0.5L_g$. In the proposed analytical threshold voltage model, z_0 is set to be 0.45 L_g for simplification.

Let $\varphi(0, z_0)$ be equal to zero; for the first-order approximation, namely only n = 1 is reserved, one obtains

$$V_{ths} = V_{FB} + \frac{qN_d}{\varepsilon_{si}} \left(\frac{L_g}{\pi}\right)^2 (1 - \alpha_1) + \frac{1}{2} \left[V_{ds} - \frac{\pi}{2} \alpha_1 \frac{\left(\frac{V_{ds} z_0}{L_g} + 2\frac{kT}{q}\right)}{\sin\left(\frac{\pi z_0}{L_g}\right)} \right] \tag{19}$$

where

$$\alpha_1 = \frac{\varepsilon_{si}}{C_{ox}}\lambda_1 I_1(R\lambda_1) + I_0(R\lambda_1) \tag{20}$$

For a long-channel device with $r_1 R \leq 1$ and$z_0 \approx L_g/2$, a second-order Taylor expansion for α_1, Eqn. (19) can be reduced to V_{thl}

$$V_{thl} = V_{FB} - \frac{qN_d R}{2C_{ox}} - \frac{qN_d R^2}{4\varepsilon_{si}} + \frac{1}{2}\left[V_{ds} - \frac{\pi}{2}(1 + \frac{R^2\pi^2}{4L_g^2} + \frac{\varepsilon_{si}R\pi^2}{2C_{ox}L_g^2})(\frac{V_{ds}}{2} + 2\frac{kT}{q})\right] \tag{21}$$

Eqn. (21) is identical to the threshold voltage for long-channel JL cylindrical surrounding-gate MOSFETs described by Eqn. (1). The deviation between them is from two reasons: different definitions of threshold voltage; the first order approximation and the effect of drain voltage are only included in Eqn. (21) whereas they are not contained in (Eqn. 1).

Figure 10 displays a comparison between the analytical results and the numerical results for the threshold voltage versus channel radius and gate length. It can be observed that the threshold voltage is very sensitive to the channel radius because the leaky path is inside the bulk instead of at the silicon/gate dielectric layer interface. This is inherently different from the conventional inversion mode MOSFETs. Moreover, the threshold voltage is reduced as the gate length decreases. This effect is known as the threshold voltage roll-off, which is a kind of typical SCEs. To effectively suppress this effect, the channel diameter should be much smaller than the gate length.

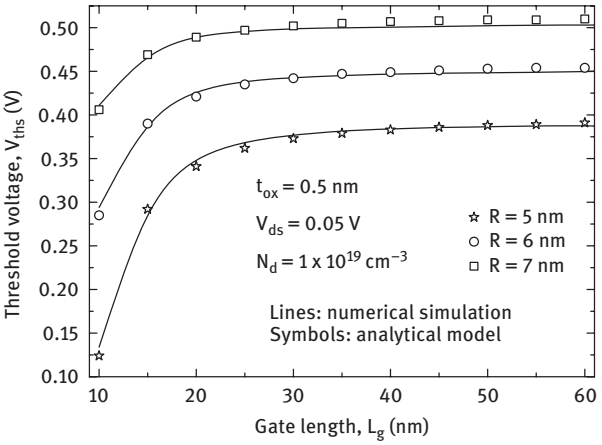

Fig. 10: Comparison of V_{th} versus channel length between the analytical model and simulation results with different radiuses. The simulated device parameters are t_{ox} = 0.5 nm, V_{ds} = 0.05 *V*, and Nd = 1 × 10¹⁹ cm^{-3}.

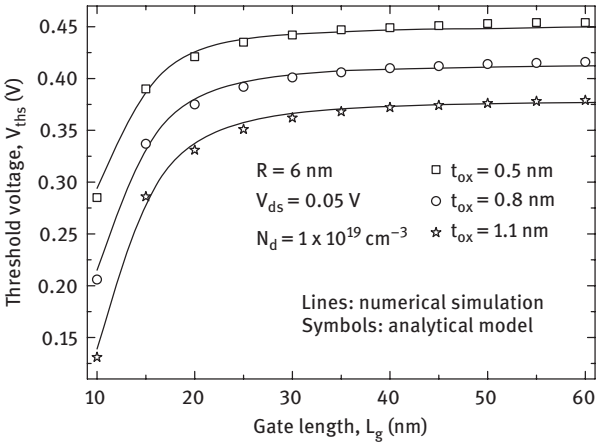

Fig. 11: Comparison of V_{th} versus channel length between the analytical model and simulation results with different equivalent oxide layer thicknesses. The simulated device parameters are R = 6 nm, V_{ds} = 0.05 V, and $N_d = 1 \times 10^{19}$ cm^{-3}.

Figure 11 displays a comparison between the analytical results and the numerical results for the threshold voltage versus equivalent oxide layer thickness and gate length. It is obvious that as t_{ox} increases, V_{ths} decreases obviously. This trend agrees with the reported results [34–37].

2.3.3 Subthreshold drain current model

Using the obtained expression of the channel potential solution, the subthreshold current density can be calculated. Gradual channel approximation (GCA) is used.

$$J(r,z) = qu_n n(r,z)\frac{d\varphi_n(z)}{dz} \tag{22}$$

where μ_n is the effective electron mobility. φ_n is the electron quasi Fermi potential, which is 0 V and V_{ds} at source end and drain end, respectively. $n(r, z)$ is the electron concentration and the distribution of electrons is assumed to be restricted to Boltzmann statistic law

$$n(r,z) = N_d \exp\left[\frac{q(\varphi(r,z) - \varphi_n - V_{ref})}{kT}\right] \tag{23}$$

Aforementioned, the drain current flows through the bulk/volume instead of the interface between the channel and the gate dielectric. Thus, the impurity scattering mechanism dominates carrier mobility degradation. Masetti model is used to