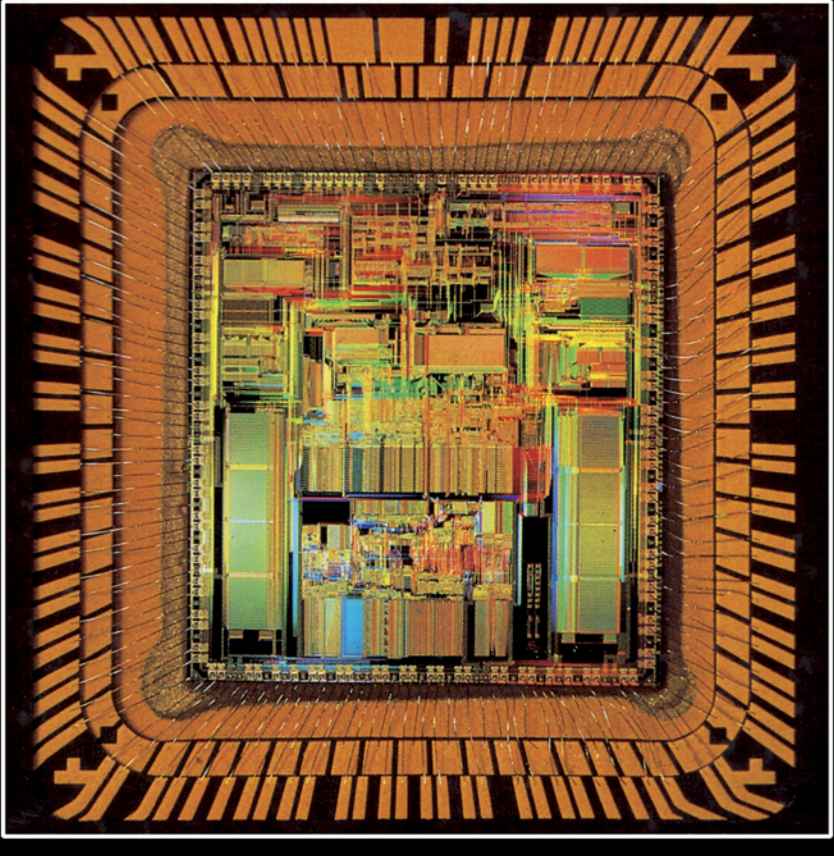
MICROPROCESSOR ARCHITECTURES AND SYSTEMS

RISC, CISC & DSP



Steve Heath

Microprocessor Architectures and Systems

This page intentionally left blank

Microprocessor Architectures and Systems

RISC, CISC and DSP

STEVE HEATH

BH NEWNES

Newnes
An imprint of Butterworth-Heinemann Ltd
Halley Court, Jordan Hill, Oxford OX2 8EJ

PART OF REED INTERNATIONAL BOOKS

OXFORD LONDON GUILDFORD BOSTON
MUNICH NEW DELHI SINGAPORE SYDNEY
TOKYO TORONTO WELLINGTON

First published 1991

British Library Cataloguing in Publication Data
Heath, Steve
Microprocessor architectures and systems : RISC, CISC and DSP.
1. Microprocessor systems. Design
I. Title
004.256

ISBN 0 7506 0032 2

Typeset by Vision Typesetting, Manchester
Printed and bound in Great Britain

For my Mother and Father
who bought me my
first soldering iron.

This page intentionally left blank

Contents

Preface

'Why are there all these different processor architectures and what do they all mean?'

'Which processor shall I use and how should I choose it?'

There has been an unparalleled introduction of new processor architectures in recent years, which has widened the choice available for designs, but has also caused much confusion with the claims and counterclaims. This has resulted in questions concerning the need for several different processor types. The struggle for supremacy between Complex Instruction Set Computer architectures and those of Reduced Instruction Set Computer purveyors and the advent of powerful Digital Signal Processors has pulled the humble microprocessor into the realm of computer architectures, where the total system is the key to understanding and successful implementations. The days of separate hardware and software engineering are now numbered because of this close interaction between hardware and software. The effect of one decision now has definite repercussions with so many aspects throughout the design.

Given the task of selecting an architecture or design approach, both engineers and managers now require a knowledge of the whole system and an explanation of the design trade-offs and their effects. Such information rarely appears within data sheets or user manuals. This book fills that knowledge gap by closely examining the developments of Motorola's CISC, RISC and DSP processors and describing the typical system configurations and engineering trade-offs that are made. The first part of the book provides a primer and history of the three basic microprocessor architectures. The second part describes the ways in which the architectures react with the system. Chapter 5 covers memory designs, memory management and cache memories. Chapter 6 examines interrupt and exception handling and the effect on real-time applications. Chapter 7 examines basic multiprocessing ideas. Chapter 8 gives some application ideas which show how certain characteristics can be exploited. The third part of the book looks at some more commercial aspects: Chapter 9 covers semiconductor technology and what it will bring, while Chapter 10 examines the changing design cycle and its implications for the design process and commercial success. Chapter 11 looks at future processor generations and Chapter 12 describes the criteria that should be examined when selecting a processor. The appendices include further information on benchmarking and binary compatibility standards.

The examples have been based around Motorola's microprocessor families, but many of the system considerations are applicable to other processors with similar architectural characteristics. The material is based on several years of involvement with users who have gone through the decision-making process and who have frequently asked the questions at the beginning of this preface. To those of you that asked and inspired this book, I thank you.

The application note on high integrity MC68020 and MC68030 designs, the descriptions of the MC68040 processor and silicon technology in Chapters 8, 9 and 11 are based on articles that I have written for *Electronic Product Design*. Their permission to reprint the material is gratefully acknowledged.

In addition, I would like to say thank you to several of my colleagues at Motorola: to Pat McAndrew who has guided and educated me through DSP, to Ronnie Sutherland and Peter Crooks who have always been willing to discuss an architectural aspect over a beer, and to John Ralston, who has always tried to achieve the impossible whenever I have asked him! Special thanks must again go to Sue Carter for yet more editing, intelligent criticism and excellent coffee and for allowing me the use of our dining room to house my computer systems.

Steve Heath

Acknowledgements

The following trademarks mentioned within the text are acknowledged:

MC6800, MC6809, MC6801, MC68000, MC68020, MC68030, MC68040, MC68332, MC68302, MC68851, MC68881, MC68882, MC68008, MC68HC000, MC68HC001, DSP56000, DSP56001, DSP96000, MC88100, and MC88200 are all trademarks of Motorola, Inc.

UNIX is a trademark of AT&T
VRTX is a trademark of Ready Systems, Inc.
OS-9 is a trademark of Microware.
pDOS is a trademark of Eyring Research.
PDP-11, VAX 11/780 and DEC are trademarks of Digital Equipment Corporation.
iAPX8086, iAPX80286, iAPX80386 are trademarks of Intel Corporation.

While the information contained in this book has been carefully checked for accuracy, the author assumes no responsibility or liability for its use, or for any infringement of patents or other rights of third parties which would result.

As technical characteristics are subject to rapid change, the data contained are presented for guidance and education only. For exact details, consult the manufacturers' data and specifications.

This page intentionally left blank

1 Complex instruction set computers

8-bit microprocessors: the precursors of CISC

Ask what the definition of a CISC (Complex Instruction Set Computer) processor is and often the reply will be based around subjective comments like 'a processor that has an over-complex and inefficient instruction set', or even simply 'an MC68000 or 8086'. The problem with these definitions is that they fail to account for the facts that more CISC microprocessors are used than any other architecture, they provide more direct hardware support for the software developer than any other architecture and are often more suitable for applications than either RISC (Reduced Instruction Set Computer) or DSP (Digital Signal Processor) alternatives. A CISC processor is better described as a mature design where software compatibility and help for software are the overriding goals. Many of today's CISC processors owe their architectural philosophy to the early 8-bit microprocessors either as a foundation or as an example of how not to design a high-performance microprocessor. It is worthwhile reviewing these early designs to act as an introduction and a backdrop to further discussions.

A microprocessor can be described simply as a data processor: information is obtained, modified according to a predetermined set of instructions and either stored or passed to other elements within the system. Each instruction follows a simple set path of fetching an instruction, decoding and acting on it, fetching data from external memory as necessary and so on. In detail, such events consist of several stages based around a single or a succession of memory accesses. Figure 1.1 shows the basic functional blocks within a typical 8-bit microprocessor. The stages needed to execute an instruction to load an accumulator with a data byte are shown in italic type. Each stage is explained below.

Start of memory cycle 1

Stage 1 Here the current program counter address is used to fetch the