STRAIN-ENGINEERED MOSFETs

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CRC Press
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CRC Press
Taylor & Francis Group
Boca Raton London New York

CRC Press is an imprint of the
Taylor & Francis Group, an **informa** business

CRC Press
Taylor & Francis Group
6000 Broken Sound Parkway NW, Suite 300
Boca Raton, FL 33487-2742

Printed in the United States of America on acid-free paper
Version Date: 2012928

International Standard Book Number: 978-1-4665-0055-6 (Hardback)

Library of Congress Cataloging-in-Publication Data

Maiti, C. K.
Strain-engineered MOSFETs / C.K. Maiti, T.K. Maiti.
p. cm.
Includes bibliographical references and index.
ISBN 978-1-4665-0055-6 (hardback)
1. Metal oxide semiconductor field-effect transistors--Reliability. 2. Integrated circuits--Fault tolerance. 3. Strains and stresses. I. Maiti, T. K. II. Title.

TK7871.99.M44M248 2012
621.3815'284--dc23 2012031209

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and the CRC Press Web site at
http://www.crcpress.com

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Preface

Microelectronics fabrication is facing serious challenges due to the introduction of new materials in manufacturing and fundamental limitations of nanoscale devices that result in increasing unpredictability in the characteristics of the devices. The downscaling of complementary metal-oxide-semiconductor (CMOS) technologies has brought about increased variability of key parameters affecting the performance of integrated circuits. In silicon-based microelectronics, technology computer-aided design (TCAD) is well established not only in the design phase but also in the manufacturing process. Device design procedures are now more challenging due to high-performance specifications, fast design cycles, and high yield requirements. Design for manufacturability and statistical design techniques are being employed to meet the challenges and difficulties of manufacturing of nanoscale-integrated circuits in CMOS technologies.

As mainstream CMOS technology is scaled below the 22 nm technology node, development of a rigorous physical and predictive compact model for circuit simulation that covers geometry, bias, temperature, DC, AC, radio frequency (RF), and noise characteristics becomes a major challenge. While introducing new device structures, innovation has always been an important part in device scaling and the integration of new materials. It is envisioned that the right combination of global biaxial and local uniaxial strain could provide additional mobility improvements at low electric fields. Written from an engineering application standpoint, the book provides the background and physical insight needed to understand new and future developments in the modelling and design of n- and p-MOSFETs at nanoscale.

Understanding predictive modelling principles to gain insight in future technology trends is important for future circuit design research and integrated circuit (IC) development. Technology CAD is a bridge between the design world and the manufacturing world. Compact models are useful not only for long-term product design but also for early evaluation of a technology for circuit manufacturing. The ultimate goal of predictive technology and process compact modelling is to describe any process technology accurately. The concepts of process compact and process technology modelling are essential to achieve the necessary knowledge transfer, which has proven to be useful in the silicon manufacturing world.

The focus of this book is on state-of-the-art MOSFETs, implemented in high-mobility substrates such as Ge, SiGe, strained Si, and ultra-thin germanium-on-insulator platforms, combined with high-k insulators and metal-gate. The book consists of 10 main chapters covering substrate-induced strain engineering in CMOS technology, process-induced stress, electronic properties of strain-engineered semiconductors, strain-engineered MOSFETs, noise in

strain-engineered devices, technology CAD and reliability of strain-engineered MOSFETs, process compact modelling, and process-aware design of strain-engineered MOSFETs, and looks beyond the 22 nm node.

Several excellent books and monographs have appeared on multigate MOSFETs, high-mobility substrates, and Ge microelectronics and strained semiconductor physics. Numerous papers have appeared on strained Si and process-induced strain, but there is a lack of a single text that combines both the strain-engineered MOSFETs and their modelling using technology computer-aided design. We attempt to summarise some of the latest efforts to reveal the advantages that strain has brought in the development of strain-engineered MOSFETs. We have included important works as well as our own research and ideas by the research community, and due to space limitations, we have referred to only representative papers and listed books recently published in related areas for additional reading.

The book is mainly meant for final-year undergraduate and postgraduate students, scientists, and engineers involved in research and development of high-performance MOSFET devices and circuits. We hope this book will help in process technology development and design of strain-engineered MOSFETs. It may also serve as a reference book on strain-engineered heterostructure MOSFETs for active researchers in this field.

We thank Chhandak Mukherjee for contributing to Chapter 6.

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About the Authors

Dr. C. K. Maiti received his BSc (Honors in Physics), B.Tech. (in Applied Physics), and M.Tech. in radiophysics and electronics from the University of Calcutta; MSc (by research) from the University of Technology in Loughborough, UK; and PhD from the Indian Institute of Technology–Kharagpur in 1969, 1972, 1974, 1976, and 1984, respectively. Dr. Maiti joined the Department of Electronics and Electrical Communication Engineering of the Indian Institute of Technology–Kharagpur in 1984 as an assistant professor and was appointed professor in 1999. He is currently the head of the department and leads the semiconductor device/process (TCAD) simulation research group within the department. He has also contributed significantly in the areas of low-temperature dielectric formation on Si, III-V semiconductors, and group IV alloy layer films. He has published four books in the silicon-germanium and strained silicon area. Dr. Maiti has edited the *Selected Works of Professor Herbert Kroemer*, published by World Scientific (Singapore, 2008). He has also served as the guest editor for the *Special Issues on Silicon-Germanium of Solid-State Electronics* (November 2001) and *Heterostructure Silicon* (August 2004). He has authored/coauthored more than 250 technical articles and conference publications. Dr. Maiti's current research interests cover various aspects of semiconductor process and device simulation of heterojunction transistors involving strained layers.

Dr. T. K. Maiti obtained his MSc degree with a gold medal in physics from Vidyasagar University, India, in 2005. In November 2005, he joined Microelectronics Centre, Indian Institute of Technology–Kharagpur, India, to carry out research work on technology CAD (TCAD) of strain-engineered MOSFETs. He completed his PhD in engineering from the Department of Electronics and Telecommunication Engineering at Jadavpur University, India, in 2009. Dr. Maiti then moved to Canada to work at McMaster University as a postdoctoral fellow on design of advanced inorganic devices (i.e., silicon, III-V, and II-VI) on silicon via modelling of the device structure, fabrication process, and electrical performances in the Engineering Physics Department from February 2010 to February 2012. Since March 2012 he has been working as a researcher at HiSIM Research Centre, Hiroshima University, Japan. Dr. Maiti's current research interests include the experimental and simulation analysis of future generation semiconductor devices as well as the development of reliable compact models for circuit and system-level simulation.

List of Abbreviations

BEOL: Back end of line
BOX: Buried oxide
BPTM: Berkeley Predictive Technology Model
BTBT: Band-to-band tunneling
BTI: Bias temperature instability
CD: Critical dimension
CESL: Contact etch stop layer
CMOS: Complementary metal-oxide-semiconductor
CMP: Chemical mechanical polishing
CVD: Chemical vapour deposition
DFM: Design for manufacturability
DFT: Density functional theory
DFY: Design for yield
DG MOSFET: Double-gate MOSFET
DIBL: Drain-induced barrier lowering
DoE: Design of experiments
DQW: Double quantum well
DRIE: Deep reactive ion etching
DSL: Dual-stress liner
e-SiGe: Embedded SiGe
EDA: Electronic design automation
EOT: Equivalent oxide thickness
EPM: Empirical pseudopotential method
EUV: Extreme ultraviolet radiation
FCC: Face-centred cubic
FEA: Finite element analysis
FEOL: Front end of line
FET: Field-effect transistor
FN: Fowler–Nordheim
FUSI: Fully silicided
GAA: Gate-all-around
GAA MOSFET: Gate-all-around MOSFET
GeOI: Germanium-on-insulator
GIDL: Gate-induced drain leakage
GR: Generation recombination
GSI: Giga-scale integration
GSMBE: Gas source molecular beam epitaxy
HBT: Heterojunction bipolar transistor
HCI: Hot-carrier injection
HDD: Highly doped drain

HFET: Heterostructure field-effect transistor
HH: Heavy hole
HK-MG: High-k/metal gate
HOT: Hybrid orientation technology
HP: High performance
IC: Integrated circuit
ITRS: International Technology Roadmap for Semiconductors
KOZ: Keep-out zone
LF: Low frequency
LH: Light hole
LNA: Low-noise amplifier
LOP: Low operating power
LRP: Limited reaction processing
LRPCVD: Limited reaction processing chemical vapour deposition
LSF: Least-squares fit
LSTP: Low standby power
MBE: Molecular beam epitaxy
MG: Metal gate
MOS: Metal-oxide-semiconductor
MOSFET: Metal-oxide-semiconductor field-effect transistor
MUGFET: Multigate MOSFET
NBTI: Negative bias temperature instability
NW: Nanowire
OMVPE: Organometallic vapour phase epitaxy
PB: Planar bulk
PBTI: Positive bias temperature instability
PCM: Process compact model
PDK: Predictive process design kit
PR: Piezoresistance
PSD: Power spectral density
PSS: Process-induced strain
PTM: Predictive technology model
QW: Quantum well
R-D: Reaction-diffusion
RBL: Relaxed buffer layer
RIE: Reactive ion etching
RPCVD: Reduced-pressure chemical vapour deposition
RTA: Rapid thermal annealing
RTCVD: Rapid thermal chemical vapour deposition
RTN: Random telegraph noise
RTS: Random telegraph signal
S/D: Source/drain
SCE: Short-channel effect
SEG: Selectively epitaxial growth
SEM: Scanning electron microscope

SEU: Single-event upset
SGOI: SiGe-on-insulator
SiGe: Silicon-germanium
SIMS: Secondary ion mass spectrometry
SMT: Stress memorisation technique
SMU: Source monitor unit
SNWT: Silicon nanowire transistor
SO: Spin-orbit
SOI: Silicon-on-insulator
SPCM: SPICE process compact model
SPT: Stress proximity technique
SQW: Single quantum well
SRB: Strain-relaxed buffer
SS: Subthreshold slope
SSDOI: Strained Si-directly-on-insulator
SSOI: Strained Si-on-insulator
STI: Shallow trench isolation
TCAD: Technology computer-aided design
TDDB: Time-dependent dielectric breakdown
TG MOSFET: Tri-gate MOSFET
TSV: Through-silicon via
UHVCVD: Ultra-high-vacuum chemical vapour deposition
ULSI: Ultra-large-scale integration
UTB: Ultra-thin body
VCO: Voltage-controlled oscillator
VLS: Vapour-liquid-solid
VLSI: Very-large-scale integration
VS: Virtual substrate
VW: Virtual wafer
VWF: Virtual wafer fabrication

List of Symbols

E: Energy
E_g: Band gap of semiconductor
E_C: Conduction band energy
E_V: Valence band energy
ΔE_C, ΔE_V: Strain-induced change in the energy of carrier subvalleys
N_C, N_V: Effective densities of states
n_i: Intrinsic carrier concentration
T_{Si}: Silicon channel thickness
t_{ox}, T_{ox}: Oxide thickness
k, k_B: Boltzmann constant
k_x, k_y, k_z: Wave vectors
W: Width of the transistor
H_{fin}: Fin height
W_{fin}: Fin width
L, Lg: Channel or gate length
V_{FB}: Flat-band voltage
V_T, V_{TH}, V_t, V_{th}: Threshold voltage
C_{ox}: Gate oxide capacitance
C_d: Depletion capacitance
Q_{ox}: Oxide charge density
ΦB: Energy difference of the Fermi level in the bulk region
V_{bi}: Built-in potential across the source/drain channel
Φ: Potential
Φ_0: Difference between the electron affinities of Si and SiO_2
ψ_s: Surface potential
μ: Mobility
μ_{eff}: Effective mobility
X_d: Channel depletion layer length
X_j: Source/drain junction depth
Q_{is}, Q_s, Q_i, N_{inv}: Inversion charge density
v: Injection velocity near source region
T: Temperature
C_L: Load capacitance
S: Subthreshold slope
f: Frequency
g_m/I_d: Transconductance-to-drain current ratio
g_m: Transconductance
$_{Vdd,}$ V_{DD}: Power supply voltage
R_{ds}: Drain/source resistance
I_{on}: On-state current

I_{off}: Off-state current
I_D, I_{DS}, I_d: Drain current of MOSFET
I_G: Gate tunneling current
V_{DS}, V_d: Drain/source voltage of MOSFET
V_{GS}: Gate/source voltage of MOSFET
R_C: Backscattering coefficient
σ: Stress
$\vec{\sigma}$: Stress tensor
F: Force
A: Area
σ_{11}, σ_{22}, σ_{33}: Normal stresses
σ_{12}, σ_{23}, σ_{13}: Shear stresses
ε: Strain
$\vec{\varepsilon}'$: Strain tensor
$\overline{S}$: Elasticity tensor
S_{11}, S_{12}, S_{44}: Parallel, perpendicular, and sheer components of elastic modulus
m^*: Conductivity effective mass
H: Hamiltonian
Ψ: Wave function
Ξ, ξ: Deformation potential
$\pi_{||}$: Longitudinal piezoresistance coefficient
$\pi_{\perp}$: Transverse piezoresistance coefficient
τ (ε): Strain relaxation time
μ_n^0, μ_P^0: Electron and hole mobility without the strain
m_{nl}, m_{nt}: Electron longitudinal and transfer masses in the subvalley
m_{Pl}, $m_{P,h}$: Hole light and heavy effective masses
F_n, F_p: Quasi-Fermi levels of electron and holes
$\psi_k(\vec{r})$, $\psi_k(\vec{r}, \varepsilon)$: Eigenfunctions for the unstrained and strained conditions
$S_I(f)$, $S_V(f)$: Current and voltage noise power spectral density
ΔN: Fluctuation in the number of carriers
τ_c, τ_e: Mean capture and emission time constants
ΔI: RTS pulse amplitude
α_H: Hooge's parameter
N_t, $N_T(E_F)$: Trap density
γ: Frequency exponent of noise
S_{ID}/I_D^2: Normalised drain current noise
λ: Tunneling attenuation length
Z_t: Position of the trap measured from the Si/SiO_2 interface
v_{TH}: Thermal velocity of electrons
σ_n: Electron capture cross section of the traps
E_T: Trap energy level
$\Delta N_{t,eff}/N_{t,eff}$: Effective change in trap density due to stress
$\Delta\Phi_B$ (σ): Ground energy-level shifts in the inversion layer for applied different types of stresses
f_t (σ): Stress-dependent trap occupation function

S_{VG} (f): Gate voltage noise power spectral density
D_{it}: Interface state density
λ_{sc}: Scattering parameter in correlated mobility fluctuation model
S_{IB}: Base current noise power spectral density
I_B: Base current
V_{BE}: Base-emitter bias voltage
V_{CE}: Collector-emitter bias voltage
A_E: Emitter area
L_S: Screening length
ΔI_B: RTS amplitude in base current
h_{21}: Current gain
S_{11}, s_{22}, s_{12}, s_{21}: S-parameters
f_T: Cutoff frequency
E_{tao}: DIBL coefficient
N_{ch}: Channel doping concentration
T_{SiN}: Nitride cap layer thickness

1

Introduction

> It is not the strongest of the species that survives, nor the most intelligent, but the one most responsive to changes.
> —Charles Darwin

In the field of microelectronics, the planar silicon metal-oxide-semiconductor field-effect transistor (MOSFET) is perhaps the most important invention. It started in 1928 when J. E. Lilienfeld proposed the concept of field-effect conductivity modulation and the MOSFET. William Shockley, John Bardeen, and Walter Brattain invented the transistor in 1947, and with the discovery of silicon dioxide (SiO_2) passivation for the Si by Atalla in 1958, the Si MOSFET era started. Since then MOSFET performance has been improved at a dramatic rate via gate length scaling, and complementary metal-oxide-semiconductor (CMOS) is currently the dominant technology for integrated circuits. As the technology scales almost every 2 years, the transistor integration capacity doubles (Moore's law), gate delay reduces by 30%, energy per logic operation reduces by 65%, and power consumption reduces by 50%. Table 1.1 shows CMOS technology outlook extrapolated from the current International Technology Roadmap for Semiconductors (ITRS) trends. However, conventional CMOS scaling has now approached the fundamental limits, which include leakage in channel and gate, diminished bulk effect, transport in silicon, and increased power dissipation. The huge costs of scaling CMOS devices according to Moore's law have now left the silicon industry at a crossroad. As technology scales, the cost of a transistor goes down, but the cost of fabrication facilities, cost of mask set, and turnaround time increase for each generation. Lithographic challenges for future technology nodes have become a major concern. Implementation of extreme ultraviolet radiation (EUV) will help continue transistor size scaling. Although it will allow for increased device density, current scaling issues will be a major concern at smaller gate length devices. ITRS 2009 has projected scaling of the advanced MOSFETs covering the next 15 years through 2022. The evolution of the Si process technology after the 130 nm node is shown in Figure 1.1. Technology challenges for 10 nm CMOS and beyond will face process limitations such as patterning ultra-fine and random features, ultra-thin gate dielectric (~3 Å), and ultra-shallow junction (~3 nm). In the following, we shall address the recent developments, which have been the subject of a major research drive for the last 10 years aimed at finding new avenues to enhance the performance of MOSFETs.

TABLE 1.1

Technology Trend

High-Volume Manufacturing	**2006**	**2008**	**2010**	**2012**	**2014**	**2016**	**2018**
Technology node	65	45	32	22	16	11	8
Integration capacity (BT)	4	8	16	32	64	128	256
Delay = CV/I scaling	~0.7	>0.7	Delay scaling will slow down	Delay scaling will slow down	Delay scaling will slow down	Delay scaling will slow down	Delay scaling will slow down
Variability	Medium	Medium	High	High	Very high	Very high	Very high

With the 90 nm technology node, strain techniques have been introduced to efficiently increase the transistor drive current by enhancing the mobility of carriers in the channel. Stress has been incorporated in MOSFETs during CMOS processing. Process-induced stress is now a viable, competitive, and important key technology that will certainly be used to boost the performance of future technology generations. Intel has been in the

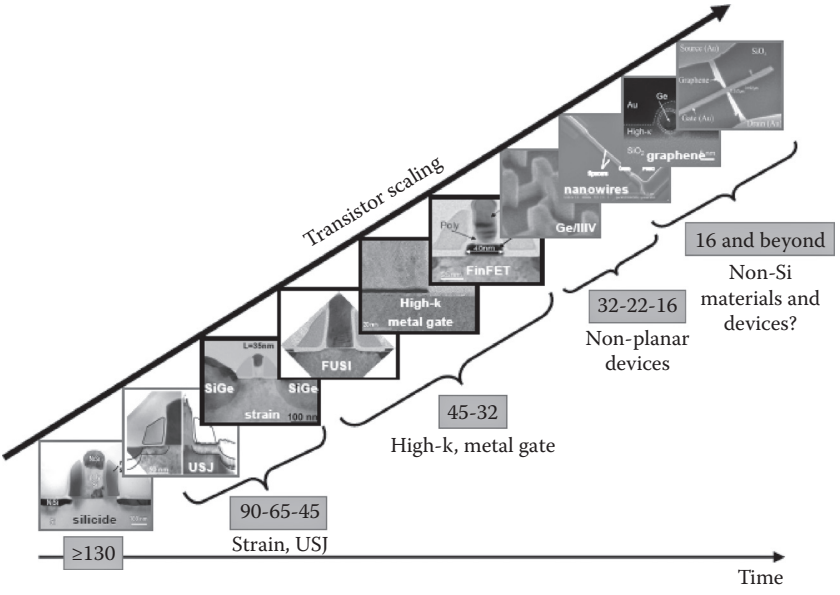

FIGURE 1.1
Evolution of the Si process technology after the 130 nm node. (After A. Shickova, Bias Temperature Instability Effects in Devices with Fully-Silicided Gate Stacks, Strained-Si, and Multiple-Gate Architectures, PhD thesis, Katholieke Universiteit-Leuven, 2008.)

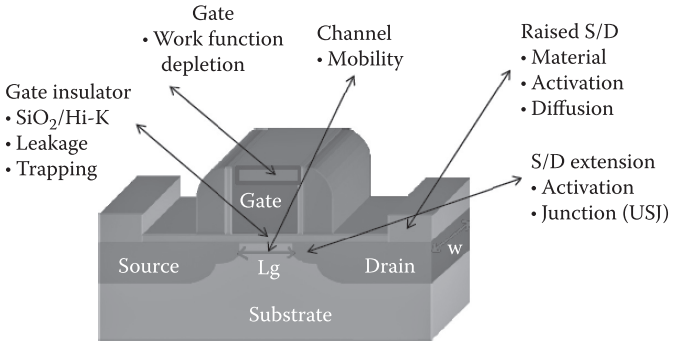

FIGURE 1.2
Main challenges for CMOS technology in 22 nm technology node. (After Maiti, T. K., Process-Induced Stress Engineering in Silicon CMOS Technology, PhD thesis, Jadavpur University, 2009.)

forefront in addressing the challenges by successfully driving transistor innovations from research phase to mainstream CMOS manufacturing. Process-induced stress engineering has kept the expectations high when Intel announced the tri-gate MOSFETs in 22 nm technology node in May 2011. The first 3D tri-gate transistor appearing at 22 nm will have a big impact on the industry. It has been predicted that the tri-gate FinFETs are both viable and capable of being tailored to suit the power/performance trade-offs for a range of applications and exceed the capabilities of present silicon-on-insulator (SOI) technology. Tri-gate FinFETs built on high-k/metal gate (HK-MG) technology, which will continue with Intel's 22 nm platform, have the flexibility for lower power consumption and much higher performance.

In scaling down CMOS technology beyond the 22 nm node, the semiconductor community will face further challenges. Figure 1.2 summarises some of the main challenges in the scaling of traditional planar bulk MOSFETs. As devices are scaled beyond the 22 nm node, various architectural and material changes in the traditional MOSFET would be required for efficient operation of the transistor. Innovative technologies such as new device architectures, mobility enhancement technology, high-k/metal gate dielectric integration, source/drain engineering, and enhanced quasi-ballistic transport channels may serve as possible solutions.

Technology development driven by Moore's law has so far played a vital role for the success of the semiconductor industry. In the last few years, the semiconductor industry has witnessed a quick development of a new area of micro- and nanoelectronics beyond the boundaries of Moore's law. The "more Moore" development is defined as a relentless scaling of digital functions and an attempt to further develop advanced CMOS technologies to reduce the cost per function. Today we have reached the end of classical Dennard scaling and are being confronted with a set of cumulative interrelated challenges at all levels, from system level down to atomic level, and require innovative

processing steps and new materials. In 2005, the strategic research agenda and vision for "more than Moore" technology had been formulated in a systematic manner by the European Technology Platform for Nanoelectronics.

1.1 Technology Scaling

In order to improve the speed of ULSI/GSI devices, new materials and device structures are being proposed. Mobility enhancement techniques such as global (substrate) strain and process-induced (local) stress are currently the most promising for improving device performance. There are a number of ways to induce strain in silicon. Different types of strain have distinct effects on electron and hole mobilities. Starting from the 90 nm technology nodes, advanced CMOS technologies feature multiple process-induced stressors such as compressive and tensile overlayers, embedded SiGe, and multiple stress memorisation techniques. Large magnitudes of uniaxial channel are being incorporated in p-MOSFETs in the 65 nm technology node, and an even higher stress level is required beyond the 22 nm technology node. Local strain approaches are based on dedicated processing steps or process modules, such as shallow trench isolation, silicidation or metal gate electrodes, the use of liners and capping layers, dry etch processes, contact etch stop layers, and source/drain engineering. Various mobility enhancement technologies currently in use are shown in Figure 1.3. Although the terms *stress* and *strain* are used very often interchangeably, they have different meanings. Stress is the force per unit area that is applied to a given material, while strain is the material response to this external stress. The stress can be accommodated in the material by changing the interatomic distances or by material expansion/contraction by defect creation.

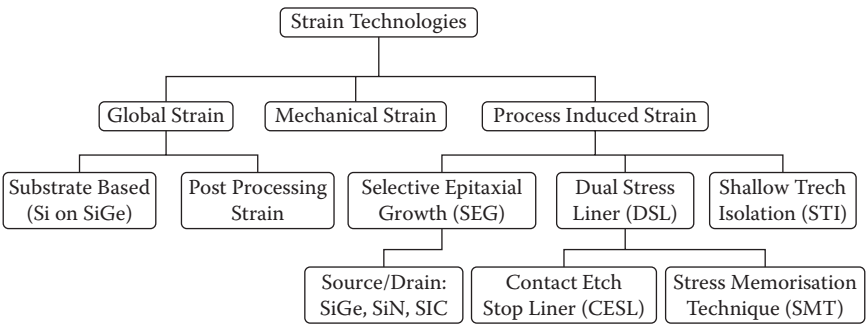

FIGURE 1.3
Different mobility enhancement technologies currently in use. (After Maiti, T. K., Process-Induced Stress Engineering in Silicon CMOS Technology, PhD thesis, Jadavpur University, 2009.)

1.2 Substrate-Induced Strain Engineering

To induce appropriate strain in the channel region of MOSFETs, various techniques have been introduced, such as substrate-induced strain, process-induced strain, and bending-induced strain. Optimisation of channel surface crystalline orientations for maximum carrier mobilities can also provide for a significant improvement in CMOS performance. Biaxial tensile silicon strain has long been known to increase electron mobility, but the strain-induced hole mobility increase is small at high vertical electric field. Substrate-induced strain engineering has become a critical feature in CMOS technology since it enhances the drain current without further gate length scaling. Recent progress has also demonstrated the evolution of the strained Si bulk MOS structure, such as the strained Si on SiGe-on-insulator (SGOI) MOSFET, and the strained Si-directly-on-insulator (SSDOI) MOSFETs. With a highly strained Si channel or a different orientation substrate in p-MOSFETs, the performance match between the n- and p-MOSFETs for CMOS applications might be achieved. Alternative channel materials with mobilities higher than silicon mobility, e.g., germanium or III-V semiconductors, can be used for device performance enhancement.

In Chapter 2, the issue of the substrates for strained-layer SiGe applications is addressed, followed by a short review of the present epitaxy techniques in use for SiGe research and production. A comprehensive review on state-of-the-art substrate-induced strain engineering methodologies in CMOS technology will be presented. Strain effect on various n- and p-channel MOSFETs in both inversion and accumulation regions are discussed. A systematic analysis of the strain effects on deeply scaled n- and p-MOSFETs with Si, SiGe, strained Si, strained Ge, and Ge channel is presented. Besides strained Si on the traditional (100) plane, it may be advantageous to change the crystal orientation to optimise CMOS circuit performance. Another way of enhancing channel mobility without the introduction of any new channel materials is the use of the hybrid crystal orientation technique. The carrier mobility of inversion layers depends on surface orientation and current flow directions, due to asymmetry of the carrier effective masses in the Si crystal lattice. Hybrid orientation technology (HOT) will also be discussed.

1.3 Process-Induced Stress Engineering

Process-induced (local) strain was first introduced into planar Si MOSFET transistors by Intel in 2002. Uniaxial strain is generated by local structural change near the channel region. The embedded SiGe (e-SiGe) under the source and drain regions resulted in larger than expected device performance

enhancement, which is attributed to compressive channel. The strain is induced by the lattice mismatch between Si and SiGe. Owing to the relative ease of integrating process-induced strain modules in conventional CMOS processing, strain-enhanced scaling is now possible. However, uniaxial channel stress requires different stress types (compressive and tensile for n- and p-MOSFETs, respectively). Stress development in integrated circuits may occur at any stage of the manufacturing process from a variety of sources that affect the device performance. Several standard processing steps can be used to introduce uniaxial strain in silicon channel for MOSFET strain engineering. Various techniques have been proposed to incorporate strain in the channel region. Most successful among these has been the introduction of SiGe in the source/drain regions, use of tensile and compressive liners, as well as the stress memorisation technique. The two critical areas of stress development in integrated circuits are (1) front-end-of-line strain-engineered channel for increasing carrier mobility and (2) thermomechanical stress development near Cu through-silicon vias (TSVs) for 3D integration. A clear understanding of the evolution of stress/strain in integrated circuits and novel ways in which it can be characterised can lead to more effective strategies to mitigate or control the stress development. Equivalent scaling strategies such as strain-engineered MOSFET channels and 3D integration schemes are important for maintaining integrated circuits performance enhancement in future semiconductor technology nodes.

In Chapter 3, typical uniaxial technologies, such as embedded or raised SiGe or SiC source/drains, Ge preamorphisation source/drain extension technology, the stress memorisation technique, and tensile or comprehensive capping layers, stress liners, and contact etch stop layers, are discussed in detail. The importance of global and local strain techniques is outlined. Layout-dependent compact modelling of mobility, velocity, and threshold voltage in strain-engineered state-of-the-art transistors using e-SiGe, dual-stress liner, and shallow trench isolation stresses are discussed. Three-dimensional integration has emerged as a viable solution to achieve higher packing density. Toward 3D integration, through-silicon vias, which directly connect stacked structures die to die, are being employed. It is important to note that the through-silicon vias (TSVs) generate a stress-induced thermal mismatch between TSVs and the silicon bulk, which affects the performance of nearby transistors, diodes, and associated circuits. Thus it is important to study the impact of TSV-induced stress on device and circuit performance. TSVs also interact with polysilicon and shallow trench isolation layout pattern density. A summary of benefits of 3D integrated circuit (ICs) and key process steps involved in their fabrication, particularly relating to through-silicon vias, will be discussed. In nanometer-scale CMOS transistors performance variability is common and layout-dependent effects have become important. The important issues of device/circuit interactions for the 22 nm node will include discussions on variability; design for manufacturing and the impact of back-end technology elements on overall device performance will also be covered.

1.4 Electronic Properties of Strained Semiconductors

The band structure provides the information about the states of energy and the electronic dispersion relation under a specific condition. It is known that if the band structure of the material is modified, mechanical and electrical properties of the material will be also changed, such as effective mass and corresponding mobility. Band structure analysis provides details about strain effects on the electron/hole transport property. For instance, strain-induced lattice constant change will induce band warping in both the conduction band and the valence band. However, the effective mass change is much more important for holes in the valence band due to a strong correlation between six subbands. In Chapter 4, we shall briefly discuss the stress–strain relationships and their effects on the band structure, and a representative method of strain components in terms of elastic compliance constants is given. The basic physical definitions, such as the strain and stress tensors, are introduced. Different methods of calculating the effect of strain on the band structure are presented. The deformation potentials of the conduction and valence bands are calculated, and the band edge shifts and splitting are discussed in detail as strain effects. Since carrier mobility is a key parameter for the simulation of the electrical characteristics of semiconductor devices, several analytical models capable of capturing the dependence of mobility on temperature, doping, and electric field will be introduced. Various types of mobility models commonly used in simulation will be described in detail.

1.5 Strain-Engineered MOSFETs

As the MOSFET channel length enters the nanometer regime, short-channel effects (SCEs), such as threshold voltage roll-off and drain-induced barrier lowering (DIBL), become high, which hinders the scaling of planar bulk or silicon-on-insulator (SOI) MOSFETs. To overcome these problems, new device architectures as well as new gate stacks have been proposed. Multigate (also known as FinFET) devices are considered a promising architecture for replacement of conventional planar MOSFETs, offering a solution for overcoming the short-channel effects and providing better threshold voltage control at short gate lengths. In Chapter 5, different schemes of multigate devices are reviewed. The tri-gate devices will be the focus of this chapter because they are a good compromise between processing complexity and electrical performance. Although the gate-all-around (GAA) and the []-gate structures show better electrical properties, they require more complex and costly processing for implementation. According to the ITRS, the strongest driver for high-k gate dielectrics comes from the need to extend

battery life for wireless devices due to lower leakage currents, which include gate leakage, subthreshold leakage, and junction leakage. Strain engineering has become a critical feature now in CMOS technology since it enhances the drain current without further gate length scaling. Process integration issues such as power consumption, leakage current, metal gate electrodes, and high-k gate dielectrics will be covered in this chapter.

1.6 Noise in Strain-Engineered Devices

Among the different types of noise mechanisms present in semiconductors, low-frequency noise, typically observed to exhibit a dependence on frequency, is very important for analogue and mixed-signal applications. Low-frequency noise is known to degrade the spectral purity of nonlinear radio frequency and microwave circuits, such as oscillators and mixers, where the low-frequency, base band noise generates noise sidebands around the radio frequency (RF) or microwave carrier signal through up conversion into unwanted phase noise. In Chapter 6, fundamental noise sources in semiconductors are reviewed and their physical origins are analytically described. The low-frequency noise is discussed as a diagnostic tool for identifying traps and defects at the insulator/semiconductor interface, and as a device lifetime prediction tool for reliability analysis. The low-frequency noise behaviour in various strain-engineered devices such as strained Si MOSFETs, multigate FETs, FinFETs, silicon nanowire transistors, and heterojunction bipolar transistors will be discussed. We shall also discuss the strain effects on MOSFET operations such as threshold voltage, gate tunneling current, and low-frequency noise characteristics. For devices processed on strained Si, it is reported that the low-frequency noise increases when Ge from the SiGe buffer diffuses up into the active layer or when threading dislocations are present. For this purpose, low-frequency noise in strained Si MOSFETs is extensively studied.

1.7 Technology CAD of Strain-Engineered MOSFETs

Technology computer-aided design (TCAD) simulations allow one to explore new technologies and novel devices through physics-based modelling, optimise process and device performance, and control manufacturing processes through statistical modelling. All these are performed on a computer and are known as virtual wafer fabrication (VWF). Basic TCAD flow is shown in Figure 1.4. Technology modelling and simulation include the semiconductor

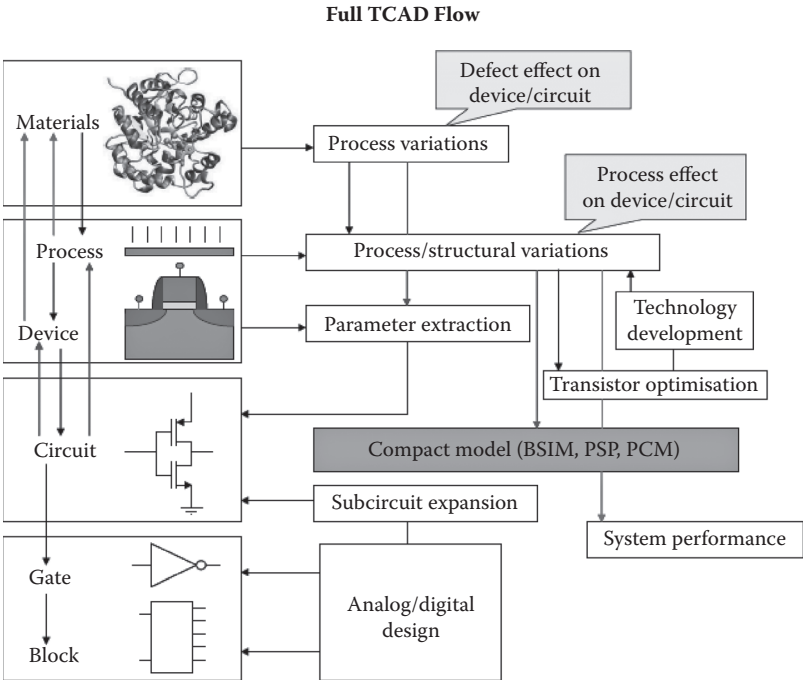

FIGURE 1.4
Compact multilevel technology/device/subsystem modelling flow. (After Maiti, T. K., Process-Induced Stress Engineering in Silicon CMOS Technology, PhD thesis, Jadavpur University, 2009.)

process modelling, and it is one of the few enabling methodologies that can reduce circuit development cycle time and cost. As the mainstream CMOS technology is scaled into the nanometer regime, development of a rigorous physical and predictive compact model for circuit simulation that covers geometry, bias, temperature, DC, AC, RF, and noise characteristics becomes a major challenge. Compact models have been at the heart of CAD tools for circuit design over the past decades, and are playing an ever increasingly important role in semiconductor manufacturing. Development of a compact model describing a new technology is essential prior to the adoption of the technology by the semiconductor industry. TCAD is currently being used for process and device design, manufacturing, and yield improvement.

Traditionally, a custom design is considered superior because it delivers higher performance and smaller die size, thus resulting in lower cost; however, this results in a longer design cycle (time to market) and is now a serious challenge for the 22 nm CMOS technology node and beyond. It is expected that the future of designs in 22 nm and beyond will be system design with design automation at all levels. Statistical fluctuations inherent in any IC manufacturing process cause variations in device and hence in circuit performance. Thus, product yield and manufacturing problems

necessitate costly redesign cycles. Technology computer-aided design is an indispensable tool for development and optimisation of new generations of electronic devices in industrial environments. Chapter 7 is dedicated to the technology CAD modelling of strain-engineered MOSFETs in process-induced strain technologies.

1.8 Reliability of Strain-Engineered MOSFETs

Scaling the conventional MOSFETs has so far been more or less a straightforward process. But the physical limitations encountered beyond the 130 nm node brought the necessity of exploration of new gate stack high-k materials, mobility enhancers, and even new device architectures. The new technologies come along with many advantages, but also raise many concerns about their reliability. Systematic studies to determine the key parameters controlling the reliability are necessary. It is important to identify the intrinsic reliability problems of the advanced devices, to distinguish them from extrinsic effects of processing, and to suggest new methods for reliability improvement. In Chapter 8, the bias temperature instabilities (BTIs) of some of the new generation devices, such as high-k/metal gate (HK-MG) stacks, strain-engineered devices with enhanced mobility, and FinFET devices, are considered. Technology CAD has been used to study the effects of strain on the negative bias temperature instabilities (NBTIs) in process-induced strained Si p-MOSFETs and hot-carrier injection in process-induced strained Si n-MOSFETs.

1.9 Process Compact Modelling

Aggressive technology scaling has led to large uncertainties in device and interconnect characteristics for deep-submicron circuits. Many physical phenomena, unforeseen in the larger dimensions, such as short-channel effect (SCE) and exponential increase in leakage, are becoming the major bottlenecks for continuous technology scaling. Increasing variations (both interdie and intradie) in device parameters (channel length, gate width, oxide thickness, device threshold voltage, etc.) produce a large spread in the delay and power consumption in advanced integrated circuits. The presence of large process variations and deep-submicron effects requires a paradigm change in the design and optimisation of large-scale circuits and systems. Innovations only in the area of technology/circuit design are not enough to combat against the different shortcomings of the process variations.