Complete PCB Design Using OrCAD® Capture and Layout

Kraig Mitzner

Containing the OrCAD® Demo Version and Design Files

Newnes

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By

Kraig Mitzner

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Introduction to Complete PCB Design Using OrCAD Capture and Layout

I did not write this book because I am an OrCAD guru. I wrote it because no up-to-date references were available when I was trying to learn how to use the software. This book is the one I wish I would have had. This book was born from notes I compiled as I learned (the hard way) to use the software. The initial intent of the book was to describe how to use OrCAD Layout specifically. Along the way, though, I realized also that I (and many of the engineers I talked to) had a lot to learn about the printed circuit board (PCB) design process itself. There was a significant amount of information available on PCB design from both the electrical and the manufacturing aspects, but there was not an easily accessible resource that covered those subjects with how to use the software. That is the intent of this book.

Chapter 1 introduces the reader to the basics of PCB design. The chapter begins by introducing the concepts of computer-aided engineering, computer-aided design, and computer-aided manufacturing. The chapter then explains how these tools are used to design and manufacture multilayer PCBs. Many 3-D pictures are used to show the construction of PCBs. Topics such as PCB cores and layer stack-up, apertures, D-codes, photolithography, layer registration, plated through-holes, and Gerber files are explained.

Chapter 2 leads new users of the software through a very simple design example. The purpose of the example is to paint a “big picture” of the design flow process. The example begins with a blank schematic page and ends with the Gerber files. The circuit is ridiculously simple so that it is not a distraction to understanding the process itself. Along the way some of Layout’s routing tools are briefly introduced along with some of the other tools, which sets the stage for Chap. 3.

Chapter 3 provides an overview of the OrCAD project files and structure and explains Layout’s tool set in detail. The chapter revisits and explains some of the actions performed and tools used during the example in Chap. 2. Gerber files are also explained in detail.

Chapter 4 introduces some of the industry standards organizations related to the design and fabrication of PCBs (e.g., IPC and JEDEC). PCB performance classes and producibility levels are also described along with the basic ideas behind standard fabrication allowances. These concepts are described here to help the reader realize some of the fabrication issues up front to help minimize board failures and to identify some of the guides and standards resources that are available for PCB design.

Chapter 5 addresses the mechanical aspect of PCB design—design for manufacturability (DFM). The chapter explains where parts should be placed on the board, how far apart, and in what orientation from a manufacturing perspective. OrCAD Layout's design rule checker is then considered relative to the manufacturing concepts and IPC's courtyard concepts. To aid in understanding the design issues, manufacturing processes such as reflow and wave soldering, pick-and-place assembly, and thermal management are discussed. The information is then used as a guide in designing plated through-holes, surface-mount lands, and Layout footprints in general. Tables summarize the information and serve as a design guide during footprint design and PCB layout.

Chapter 6 addresses the electrical aspect of PCB design. There are several good references available on signal integrity, electromagnetic interference, and electromagnetic compatibility. Chapter 6 provides an overview of those topics and applies them directly to PCB design. Topics such as loop inductance, ground bounce, ground planes, characteristic impedance, reflections, and ringing are discussed. The idea of "the unseen schematic" (the PCB layout) and its role in circuit operation on the PCB is introduced. Look-up tables and equations are provided to determine required trace widths for current handling and impedance as well as required trace spacing for high-voltage designs and high-frequency designs. Various layer stack-up topographies for analog, digital, and mixed-signal applications are also described. The design examples in Chap. 9 demonstrate how to apply the layer stack-ups described in this chapter.

Chapter 7 explains how to construct Capture parts using the Capture Library Manager and Part Editor and the PSpice Model Editor. Heterogeneous and homogeneous parts are developed in examples using four different methods. Different methods are used depending on whether a part will be used for simple schematic entry, design projects intended for PCB layout, PSpice simulations, or all of the above. The chapter also demonstrates how to attach PSpice models to Capture's schematic parts using PSpice models downloaded from the Internet and basic PSpice models developed from functional Capture projects. The Capture parts can then be used for both PSpice simulations and PCB layout as demonstrated in Chap. 9.

Detailed coverage of padstacks and footprints is covered in Chap. 8. The chapter introduces the Layout Library Manager, Layout's footprint naming conventions, and the basic composition of a footprint. Then a detailed description of the padstack (as it relates to PCB manufacturing described in Chaps. 1 and 5) is given, as it is the foundation of both footprint design and PCB routing. Design examples are provided to demonstrate how to design discrete through-hole and surface-mount devices and how to use the pad array generator to design footprints for pin grid arrays and ball grid arrays with dogbone fanouts included with the footprint.

Chapter 9 provides four PCB design examples that use the material covered in the previous eight chapters. The first example is a simple analog design using a single op-amp. The design shows how to set up multiple plane layers for positive and negative power supplies and ground. The design also demonstrates several key concepts in Capture, such as how to connect global nets, how to assign footprints, how to perform design rule checks, how to

use the Capture part libraries, how to generate a bill of materials (BOM), and how to use the BOM as an aid in the design process in Capture and Layout. The design also shows how to perform important tasks in Layout such as how to load board technology files, locate specific parts, and modify padstacks. Intertool communication (such as annotation and back annotation) between Capture and Layout is also demonstrated. The second design is a mixed digital/analog circuit. In addition to the tasks demonstrated in the first example, the design also demonstrates how to set up and use split planes to isolate analog and digital power supplies and grounds. Other tasks include using copper pours on routing layers to make partial ground planes, using copper pours on plane layers to make nested power and ground planes, and defining anti-copper areas on plane and routing layers. The third example uses the same mixed digital/analog circuit from the second example but demonstrates how to use multiple page schematics and off-page connectors to add PSpice simulations to a Capture project used for PCB layout, all within a single project design. It also demonstrates how to construct multiple, separated power and ground planes and a shield plane to completely isolate analog from digital circuitry. The use of guard rings and guard traces is also demonstrated. The fourth example is a high-speed digital design, which demonstrates how to design transmission lines, stitch multilayer ground planes, perform pin/gate swapping, place moated ground areas for clock circuitry, and design a heat spreader.

Chapter 10 describes how to postprocess a PCB design and generate specific Gerber files. Through an example it is shown how to relate the OrCAD Layout design perspective and layer stack-up (including image polarity) to the board manufacturer's perspective by submitting Gerber files to an actual board manufacturer via the Internet. The discussion also provides an example fabrication quote. Nonstandard Gerber files are briefly discussed as well as Gerber files that are generated for PCBs with nonplated mounting holes.

Chapter 11 introduces other tools that can be used with OrCAD Capture and Layout to enhance the PCB design process. The chapter provides examples of how to use Microsoft Excel with the bill of materials generated by Capture to create parts lists and various other tracking documents that can be used during the PCB layout process to minimize design errors. Other examples include how to use PSpice to simulate transmission lines to aid in circuit design and PCB layout, how to use the SPECCTRA autorouter with Layout to route high-density PCB designs faster and with less manual cleanup, how to use GerbTool to panelize a board design, and how to use Layout to generate a .DXF file that can be used by a graphics program to construct a 3-D image of your board design. The IPC Land Pattern Viewer is also introduced in this chapter.

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CHAPTER 1

Introduction to PCB Design and CAD

Computer-Aided Design and the OrCAD Design Suite

Before digging into the details of Layout, we will take a moment to discuss computer-aided engineering (CAE) tools in general. Computer-aided engineering tools cover all aspects of engineering design from drawings to analysis to manufacturing. Computer-aided design (CAD) is a category of CAE that is related to the physical layout and drawing development of a system design. CAD programs specific to the electronics industry are known as electronic CAD (ECAD) or electronic design automation (EDA). EDA tools reduce development time and cost because they allow designs to be simulated and analyzed prior to purchasing and manufacturing hardware. Once a design has been proven through drawings, simulations, and analysis, the system can be manufactured. Applications used in manufacturing are known as computer-aided manufacturing (CAM) tools. CAM tools use software programs and design data (generated by the CAE tools) to control automated manufacturing machinery to turn a design concept into reality.

So how does OrCAD/Cadence fit into all of this? Cadence owns and manages many types of CAD/CAM products related to the electronics industry, including the OrCAD design suite. The OrCAD design suite can be purchased through resellers such as EMA Design Automation, Inc., who package different combinations of CAD/CAM applications, including Capture, PSpice, and Layout, to suit customers' needs. Although these applications can operate individually, bundling the individual tools into one suite allows for intertool communication. The OrCAD tools can also interact with other CAD/CAM tools such as GerbTool, SPECCTRA, or Allegro. Chapter 11 covers the use of these tools with OrCAD.

Capture is the centerpiece of the package and acts as the prime EDA tool. Capture contains extensive parts libraries that may be used to generate schematics that stand alone or that interact with PSpice, or Layout, or both simultaneously. A representation of a Capture part is shown in Fig. 1-1. The pins on a Capture part can be mapped into the pins of a PSpice model and/or the pins of a physical package in Layout. PSpice is a CAE tool that contains the mathematical models for performing simulations, and Layout is a CAD tool that converts a symbolic schematic diagram into a physical representation of the design. Netlists are used to interconnect parts within a design and connect each of the parts with its model and footprint. In addition to being a CAD tool, Layout also functions as a front-end CAM tool by generating the data on which other CAM

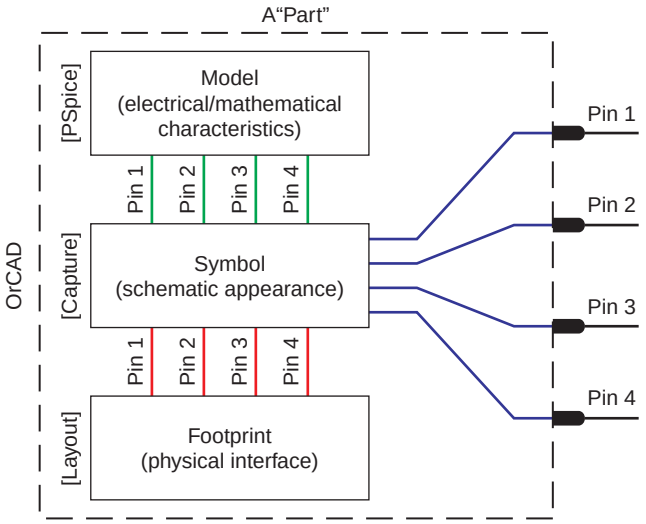

Figure 1-1 The pieces of a “part.”

tools operate when manufacturing the printed circuit board (PCB) (GerbTool, for example). By combining all three applications into one package you have a powerful set of tools to efficiently design, test, and build electronic circuits. The key to successful project design and production is in understanding the PCB itself and knowing how to use the tools that build the PCB.

Printed Circuit Board Fabrication

We now look at how PCBs are manufactured so that we will have a better understanding of what we are trying to accomplish with Layout and why. A PCB consists of two basic parts: a substrate (the board) and printed wires (the copper traces). The substrate provides a structure that physically holds the circuit components and printed wires in place and provides electrical insulation between conductive parts. A common type of substrate is FR4, which is a fiberglass–epoxy laminate. It is similar to older types of fiberglass boards but is flame resistant. Substrates are also made from Teflon, ceramics, and special polymers.

PCB cores and layer stack-up

During manufacturing the PCB starts out as a copper clad substrate as shown in Fig. 1-2. A rigid substrate is a C-stage laminate (fully cured epoxy). The copper cladding may be copper that is plated onto the substrate or copper foil that is glued to the substrate. The thickness of the copper is measured in ounces (oz) of copper per square foot, where 1.0 oz/ft^2 of copper is approximately 1.2–1.4 mils (0.0012–0.0014 in.) thick. It is common to drop “/ft^2” and refer to the thickness only in oz. For example, you can order 1 oz copper on a $\frac{1}{8}$-in.-thick FR4 substrate.

A substrate can have copper on one or both sides. Multilayer boards are made up of one or more single- or double-sided substrates called cores. A core is a copper-plated epoxy laminate. The cores are glued together with one or more sheets of a partially cured epoxy as shown in

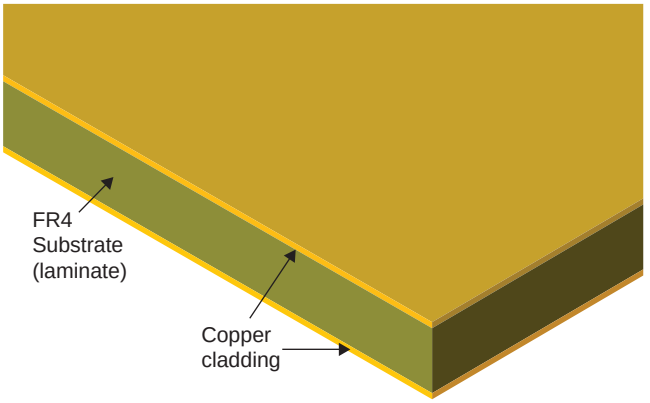

Figure 1-2 A double-sided copper clad FR4 substrate.

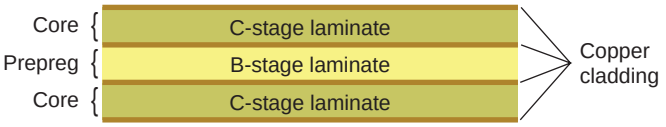

Figure 1-3 Cores and prepreg.

Fig. 1-3. The sheets are also referred to as prepreg or B-stage laminate. Once all of the cores are patterned (described below) and aligned, the entire assembly is fully cured in a heated press.

There are three methods of assembling the cores when making a multilayer board. Figure 1-4 shows the first two methods in an example with four routing layers and two plane layers. Figure 1-4(a) shows three (double-sided) cores bonded together by two prepreg layers, while Fig. 1-4(b) shows the same six layers made of two cores, which make up the four inner layers, bonded together by one prepreg layer. The outer layers in 1-4(b) are copper foil sheets bonded to the assembly with prepreg.

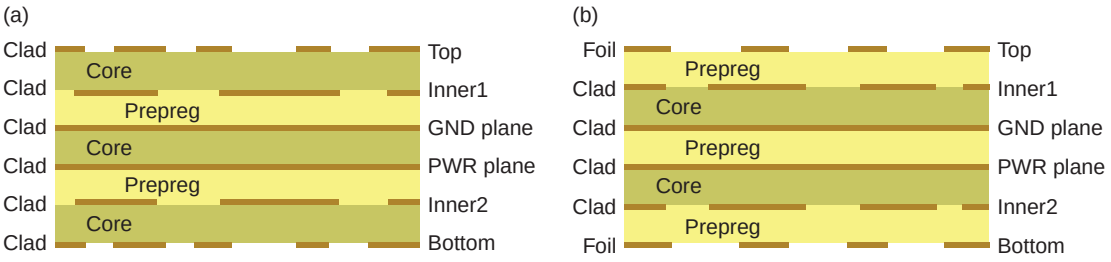

Figure 1-4 Two stack-up methods for a six-layer board. (a) Multicore, outer clad. (b) Multicore, outer foil.

The routing layers in Fig. 1-4 are shown as patterned copper segments and the plane layers are shown as solid lines. The inner layers are patterned prior to bonding the cores together. The outer layers are patterned later in the process after the cores have been bonded and cured and most of the holes have been drilled. Because the outer layers are etched later and because copper foil is typically less expensive than copper cladding, the stack-up shown in Fig. 1-4(b) is more widely used.

The third method uses several fabrication techniques by which highly complex boards can be fabricated, as illustrated in Fig. 1-5. This circuit board may have a typical four-layer core stack-up at its center, but additional layers are built up layer by layer on the top and the bottom using sequential lamination techniques. The techniques can be used to produce blind and buried vias as well as typical plated through-hole vias and nonplated holes. Resistors and capacitors can also be embedded into the substrate. More will be discussed about blind vias in later chapters (8 and 9).

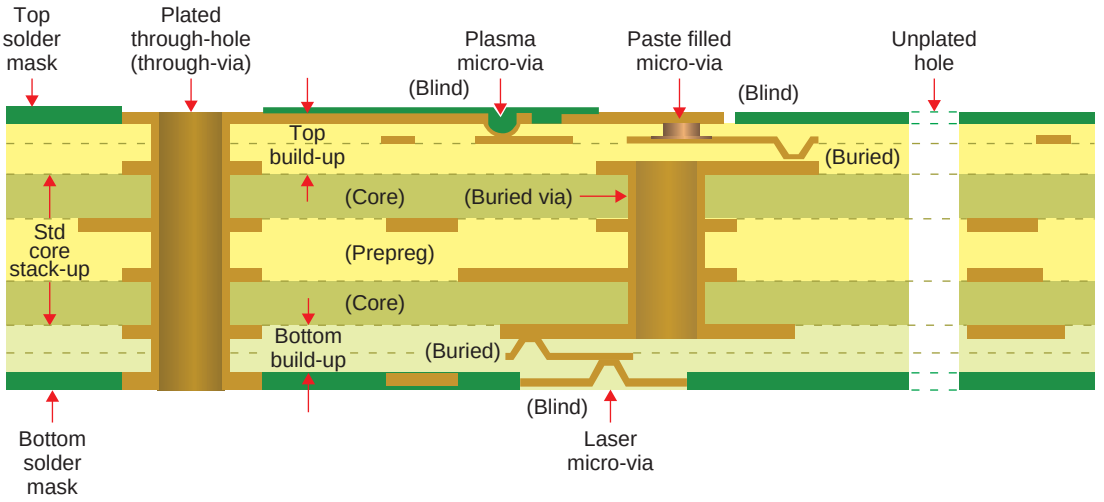

Figure 1-5 A built-up, multitechnology, PCB stack-up.

PCB fabrication process

The copper traces and pads you see on a PCB are produced by selectively removing the copper cladding and foil. There are two common methods for removing the unwanted copper: wet acid etching and mechanical milling. Acid etching is more common when manufacturing large quantities of boards because many boards can be made simultaneously. One drawback to wet etching is that the chemicals are hazardous and must be replenished occasionally, and the depleted chemicals must be recycled or discarded. Milling is usually used for smaller production runs and prototype boards. During milling, the traces and pads are formed by a rotating bit that grinds the unwanted copper from the substrate. With either method, a digital map is made of the copper patterns. The purpose of CAD software like OrCAD Layout is to generate the digital maps.

Note

- *Only one layer is considered in the following explanation of the fabrication process.*

Photolithography and chemical etching

Selectively removing the copper with etching processes requires etching the unwanted copper while protecting the wanted copper from the etchant. This protection is provided by a polymer coating (called photoresist) that is deposited onto the surface of the copper cladding as shown in Fig. 1-6. The photoresist is patterned into the shape of the desired printed circuit through a process called photolithography. The patterned resist protects selected areas of the copper from the etchant and exposes the copper to be etched.

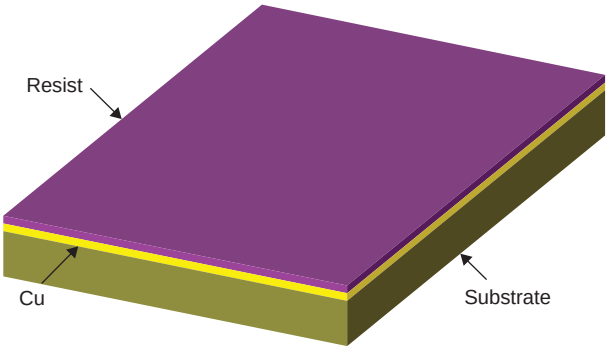

Figure 1-6 A copper clad board coated with photoresist.

There are two steps to photolithography, patterning the photoresist—exposing the resist to light (typically ultraviolet (UV) light) and developing it (selective removal in a chemical bath). There are two types of photoresist: positive resist and negative resist. When positive resist is exposed to UV light, the polymer breaks down and can be removed from the copper. Conversely, negative resist that is shielded from UV light is removed.

A mask is used to expose the desired part of the photoresist. A mask is a specialized black and white photographic film or glass photoplate on which a picture of the traces and pads is printed with a laser photoplotter. Two types of masks are shown in Fig. 1-7. The masks are examples of a trace connected to a pad. Figure 1-7(a) shows a positive mask used to expose positive photoresist, and Fig. 1-7(b) shows a negative mask used to expose negative photoresist. Masks that will be used repeatedly are sometimes produced on glass photoplates instead of film.

The mask is placed on top of the photoresist as shown in Fig. 1-8, and the assembly is exposed to the UV light. The dark areas block UV light and the white (transparent) areas allow the UV light to hit the photoresist, which imprints the circuit image into the photoresist. A separate mask is used for each layer of a circuit board. OrCAD Layout generates the data that the photoplotter uses to make these masks.

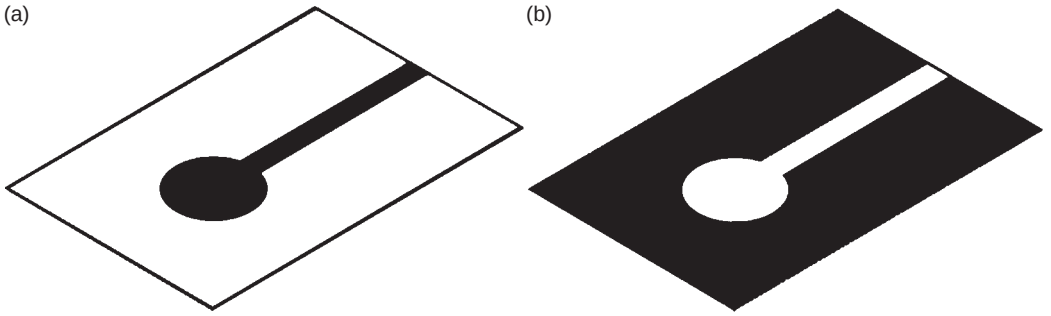

Figure 1-7 Photolithography masks. (a) A positive mask. (b) A negative mask.

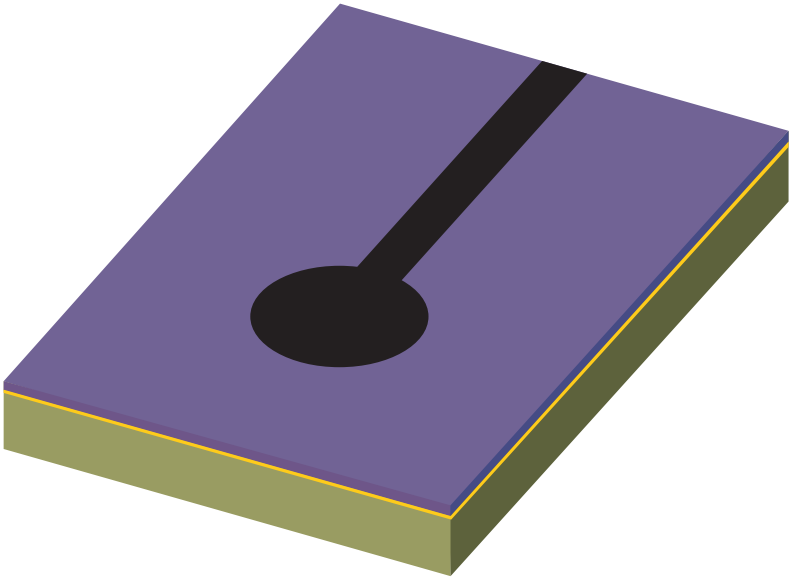

Figure 1-8 Positive photomask on photoresist-coated board.

Another way of exposing the photoresist is by using a programmable laser to "draw" the pattern directly onto the photoresist. This is a newer technique called laser direct imaging (LDI). A benefit of the LDI process is that it uses the same data as the photoplotters but no masks are required.

After the photoresist has been exposed (either with the mask and UV or with the laser) it is washed in a chemical called the developer. In the case of positive resist, the resist breaks down during exposure and is removed by the developer. In the case of negative resist, the UV light cures the resist, and only the unexposed resist is removed by the developer. Common developers are sodium hydroxide (NaOH) for positive resist and sodium carbonate (Na_2CO_3) for negative resist. Once the resist has been exposed and developed, a circuit image made of the photoresist is left on the copper as shown in Fig. 1-9.